

ABOV SEMICONDUCTOR Co., Ltd.
Universal Asynchronous
Receiver/Transmitter with FIFOs

MC16C550

User's Manual (Ver. 1.06)



REVISION HISTORY (I)

VERSION 1.06 (May 23, 2008) add package type in features

VERSION 1.05 (May 19, 2008) change AC characteristics

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Version 1.06

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MC16C550

Universal Asynchronous

Receiver/Transmitter with FIFOs

1. OVERVIEW

1.1 Description

The MC16C550 is an improved version of the original 16450 Universal Asynchronous Receiver/Transmitter (UART). Functionally identical to the 16450 on power up (CHARACTER mode)* the MC16C550 can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead.

In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signaling of DMA transfers.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16}-1$), and producing a $16 \times$ clock for driving the internal transmitter logic. Provisions are also included to use this $16 \times$ clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

*Can also be reset to 16450 Mode under software control.

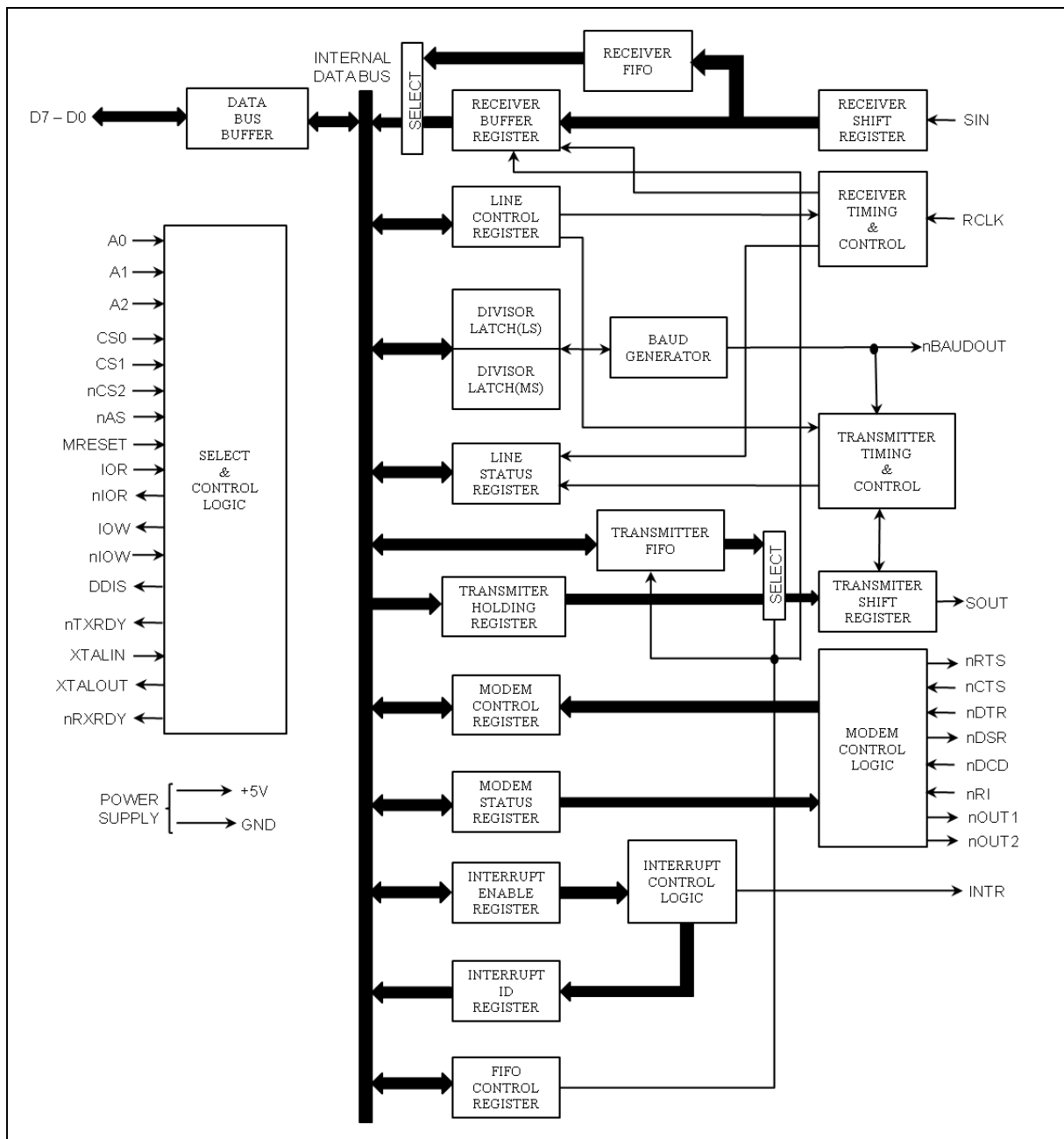
1.2 Features

- 3.3 to 5V operation
- Capable of running all existing 16450 software.
- Pin for pin compatible with the existing 16450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins are nTXRDY and nRXRDY, respectively.
- After reset, all registers are identical to the 16450 register set.
- In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data.
- Holding and shift registers in the 16450 Mode eliminate the need for precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to ($2^{16} - 1$) and generates the $16 \times$ clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
 - 5-, 6-, 7-, or 8-bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1-, $1\frac{1}{2}$ -, or 2-stop bit generation
 - Baud generation (DC to 256K baud).
- False start bit detection.
- Complete status reporting capabilities.
- Line break generation and detection.
- Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation
 - Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.

Ordering Information

Device name	Package
MC16C550B	40 DIP
MC16C550P	44 PLCC
MC16C550L	48 LQFP

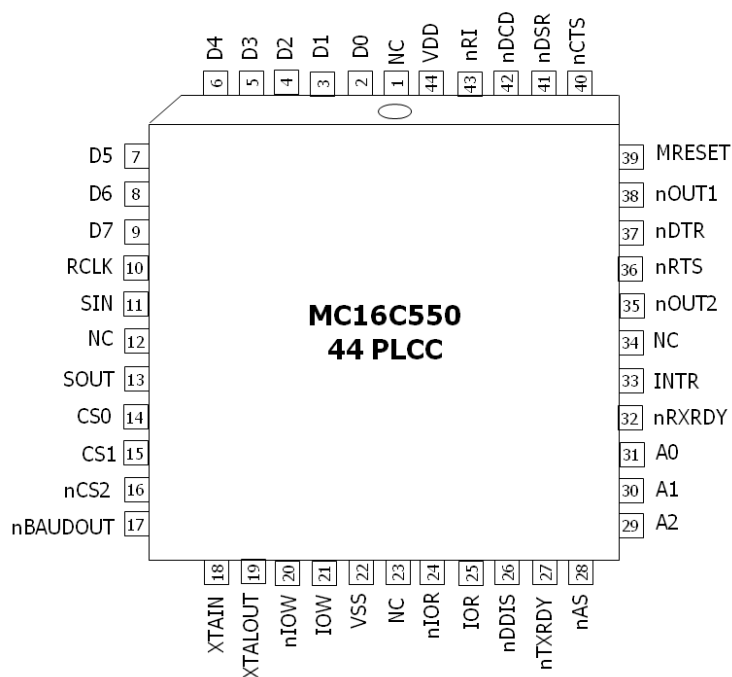
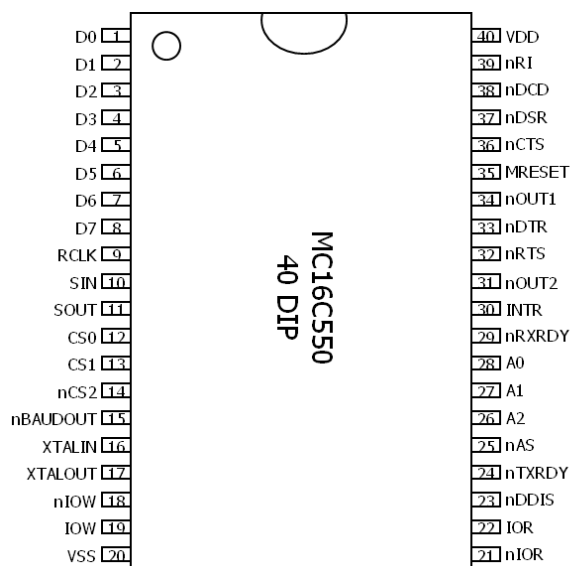
2. BLOCK DIAGRAM

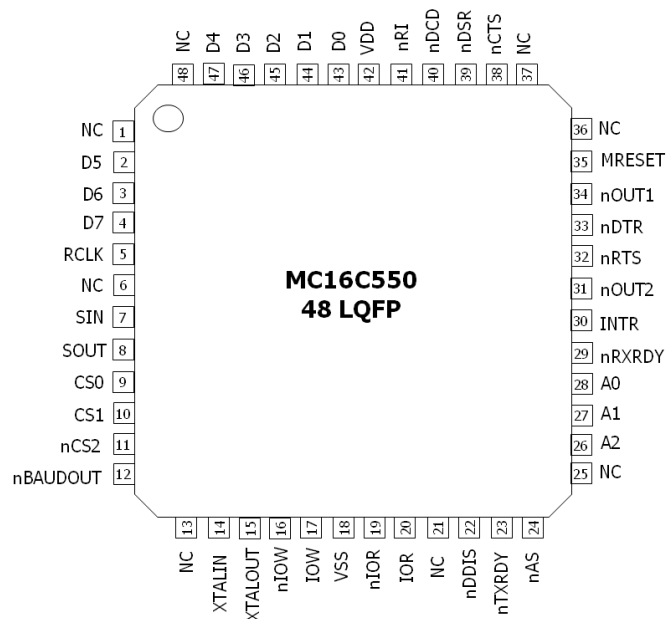


3. PIN ASSIGNMENT

PIN	40 DIP	44 PLCC	48 LQFP
1	D0	NC	NC
2	D1	D0	D5
3	D2	D1	D6
4	D3	D2	D7
5	D4	D3	RCLK
6	D5	D4	NC
7	D6	D5	SIN
8	D7	D6	SOUT
9	RCLK	D7	CS0
10	SIN	RCLK	CS1
11	SOUT	SIN	nCS2
12	CS0	NC	nBAUDOUT
13	CS1	SOUT	NC
14	nCS2	CS0	XTALIN
15	nBAUDOUT	CS1	XTALOUT
16	XTALIN	nCS2	nIOW
17	XTALOUT	nBAUDOUT	IOW
18	nIOW	XTALIN	VSS
19	IOW	XTALOUT	nIOR
20	VSS	nIOW	IOR
21	nIOR	IOW	NC
22	IOR	VSS	nDDIS
23	nDDIS	NC	nTXRDY
24	nTXRDY	nIOR	nAS
25	nAS	IOR	NC
26	A2	nDDIS	A2
27	A1	nTXRDY	A1
28	A0	nAS	A0
29	nRXRDY	A2	nRXRDY
30	INTR	A1	INTR
31	nOUT2	A0	nOUT2
32	nRTS	nRXRDY	nRTS
33	nDTR	INTR	nDTR
34	nOUT1	NC	nOUT1
35	MRESET	nOUT2	MRESET
36	nCTS	nRTS	NC
37	nDSR	nDTR	NC
38	nDCD	nOUT1	nCTS
39	nRI	MRESET	nDSR
40	VDD	nCTS	nDCD
41		nDSR	nRI
42		nDCD	VDD
43		nRI	D0
44		VDD	D1
45			D2
46			D3
47			D4
48			NC

4. PACKAGE DIAGRAM





5. PIN FUNCTION

The following describes the function of all UART pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 and a high represents a logic 1.

A0, A1, A2, Register Select: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Register Address				Register
DLAB	A ₂	A ₁	A ₀	
0	0	0	0	Receiver Buffer(read) Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
x	0	1	0	Interrupt Identification(read)
x	0	1	0	FIFO Control
x	0	1	1	Line Control
x	1	0	0	MODEM Control
x	1	0	1	Line Status
x	1	1	1	MODEM Status
x	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

nAS, Address Strobe: The positive edge of an active Address Strobe (nAS) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, nCS2) signals.

Note: An active nAS input is required when the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, nCS2) signals are not stable for the duration of a read or write operation. If not required, tie the nAS input permanently low.

nBAUDOUT, Baud Out: This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The nBAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

CS0, CS1, nCS2, Chip Select: When CS0 and CS1 are high and nCS2 is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If nAS is always low, valid chip selects should stabilize according to the t_{CSW} parameter.

nCTS, Clear to Send: When low, this indicates that the MODEM or data set is ready to exchange data.

The nCTS signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the nCTS signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the nCTS input has changed state since the previous reading of the MODEM Status Register. nCTS has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

D7-D0, Data Bus: This bus comprises eight TRISTATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

nDCD, Data Carrier Detect: When low, indicates that the data carrier has been detected by the MODEM or data set. The nDCD signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the nDCD signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the nDCD input has changed state since the previous reading of the MODEM Status Register. nDCD has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

nDDIS, Driver Disable: This goes low Whenever the CPU is reading data from the UART.

It can disable or control the direction of a data bus transceiver between the CPU and the UART.

nDSR, Data Set Ready: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The nDSR signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the nDSR signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the nDSR input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DDSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

nDTR, Data Terminal Ready: When low, this informs the MODEM or data set that the UART is ready to establish a communications link.

The nDTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

INTR, Interrupt: This pin goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTR signal is

reset low upon the appropriate interrupt service or a Master Reset operation.

MRESET, Master Reset: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, nOUT 1, nOUT 2, nRTS, nDTR) are affected by an active MRESET input (Refer to Table I.) This input is buffered with a CMOS compatible Schmitt Trigger with 0.5V typical hysteresis.

nOUT 1, Output 1: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

nOUT 2, Output 2: This user-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state.

Loop mode operation holds this signal in its inactive state.

RCLK, Receiver Clock: This input is the 16 × baud rate clock for the receiver section of the chip.

IOR, nIOR, Read: When IOR is high or nIOR is low while the chip is selected, the CPU can read status information or data from the selected UART register.

Note: Only an active IOR or nIOR input is required to transfer data from the UART during a read operation. Therefore, tie either the IOR input permanently low or the nIOR input permanently high, when it is not used.

nRI, Ring Indicator: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The nRI signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the nRI signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the nRI input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

nRTS, Request to Send: When low, this informs the MODEM or data set that the UART is ready to exchange data. The nRTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

SIN, Serial Input: Serial data input from the Communications link (peripheral device, MODEM, or data set).

SOUT, Serial Output: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking

(logic 1) state upon a Master Reset operation.

nTXRDY, nRXRDY: Transmitter and Receiver DMA signaling is available through two pins. When operating in the FIFO mode, one of two types of DMA signaling per pin can be selected via FCR3. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi transfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled.

RXRDY, Mode 0: When in the 16450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) and there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY pin (29) will be low active. Once it is activated the RXRDY pin will go inactive when there are no more characters in the FIFO or holding register.

RXRDY, Mode 1: In the FIFO Mode (FCR0=1) when the FCR3=1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.

TXRDY, Mode 0: In the 16450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) and there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY pin (24) will be low active. Once it is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO or holding register.

TXRDY, Mode 1: In the FIFO Mode (FCR0=1) when FCR3=1 and there are no characters in the XMIT FIFO, the TXRDY pin will go low active. This pin will become inactive when the XMIT FIFO is completely full.

VDD: +3.3V or 5V supply.

VSS: Ground (0V) reference.

IOW, nIOW, Write: When IOW is high or nIOW is low while the chip is selected, the CPU can write control words or data into the selected UART register.

Note: Only an active IOW or nIOW input is required to transfer data to the UART during a write operation. Therefore, tie either the IOW input permanently low or the nIOW input permanently high, when it is not used.

XTALIN (External Crystal Input): This signal input is used in conjunction with XTALOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal will be generated off-chip, then it should drive the baud rate generator through this pin.

XTALOUT (External Crystal Output): This signal output is used in conjunction with XTALIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal will be generated off-chip, then this pin is unused.

TABLE 1. UART Reset Configuration

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	0000 0000 (Note 1)
Interrupt Identification Register	Master Reset	0000 0001
FIFO Control	Master Reset	0000 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	0000 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
nOUT 2	Master Reset	High
nRTS	Master Reset	High
nDTR	Master Reset	High
nOUT 1	Master Reset	High
RCVR FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low

Note 1: Boldface bits are permanently low.

Note 2: Bits 7-4 are driven by the input signals.

6. Electrical CHARACTERISTICS

6.1 Absolute Maximum Ratings

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to GND	-0.5V to +7.0V
Power Dissipation	500mW

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

6.2. DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V}$ or $5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise specified

Symbol	Parameter	3.3V		5V		Units	Conditions
		Min	Max	Min	Max		
V_{ILX}	Clock Input Low Voltage	-0.3	$0.3 V_{DD}$	-0.3	$0.3 V_{DD}$	V	
V_{IHX}	Clock Input High Voltage	$0.7 V_{DD}$	$V_{DD}+0.3$	$0.7 V_{DD}$	$V_{DD}+0.3$	V	
V_{IL}	Input Low Voltage	-0.3	$0.3 V_{DD}$	-0.3	$0.3 V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7 V_{DD}$	$V_{DD}+0.3$	$0.7 V_{DD}$	$V_{DD}+0.3$	V	
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	$I_{OL} = 1.6\text{ mA}$ on all, Note 1
V_{OH}	Output High Voltage	$V_{DD}-0.4$	-	$V_{DD}-0.4$	-	V	$I_{OH} = -1.0\text{ mA}$, Note 1
$I_{CC}(\text{AV})$	Average Power Supply Current (V_{DD})	-	4.5 (Note 2)	-	10 (Note 2)	mA	$V_{DD} = V_{DD\text{ max}}$, No loads on output SIN, DSR, DCD, CTS (Note 3)
I_{IL}	Input Leakage	-	± 1	-	± 1	μA	$V_{DD} = V_{DD\text{ max}}$, $V_{SS} = 0\text{V}$ All other pins floating $V_{IN} = 0\text{V}$, $V_{DD\text{ max}}$ (Note 3)
I_{CL}	Clock Leakage	-	± 1	-	± 1	μA	
V_{ILMR}	MR Schmitt V_{IL}	-	$0.2 V_{DD}$	-	$0.2 V_{DD}$	V	
V_{IHMR}	MR Schmitt V_{IH}	$0.8 V_{DD}$	-	$0.8 V_{DD}$	-	V	

Note 1. Does not apply to XTALOUT.

Note 2. $T_A = 25^\circ\text{C}$

Note 3. $V_{DD\text{ max}} = 3.6\text{V}$ ($V_{DD}=3.3\text{V}$) or 5.5V ($V_{DD}=5.0\text{V}$)

Capacitance $T_A = 25^\circ\text{C}$, $V_{DD} = V_{SS} = 0\text{V}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{XIN}	Clock input Capacitance		15	20	pF	$f_C = 1\text{MHz}$
C_{OUT}	Clock output Capacitance		20	30	pF	Unmeasured pins
C_{IN}	Input Capacitance		6	10	pF	Returned to V_{SS}
C_{OUT}	Output Capacitance		10	20	pF	

6.3. AC Characteristics $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V}$ or $5\text{V} \pm 10\%$

Symbol	Parameter	Min	Max	Units	Conditions
t_{ADS}	Address Strobe Width	60		ns	
t_{AH}	Address Hold Time	0		ns	
t_{AR}	IOR, nIOR Delay from Address	30		ns	Note 1
t_{AS}	Address Setup Time	60		ns	
t_{AW}	nIOW, IOW Delay from Address	30		ns	Note 1
t_{CH}	Chip Select Hold Time	0		ns	
t_{CS}	Chip Select Setup Time	60		ns	
t_{CSR}	nIOR, IOR Delay from Chip Select	30		ns	Note 1
t_{CSW}	nIOW, IOW Delay from Select	30		ns	Note 1
t_{DH}	Data Hold Time	30		ns	
t_{DS}	Data Setup Time	30		ns	
t_{HZ}	nIOR, IOR to Floating Data Delay	0	100	ns	100 pF loading, Note 3
t_{MR}	Master Reset Pulse Width	20		ns	
t_{RA}	Address Hold Time from nIOR, IOR	20		ns	Note 1
t_{RC}	Read Cycle Delay	125		ns	
t_{RCS}	Chip Select Hold Time from nIOR, IOR	20		ns	Note 1
t_{RD}	nIOR, IOR Strobe Width	125		ns	
t_{RDD}	nIOR, IOR to Driver Enable/Disable		60	ns	100 pF loading, Note 3
t_{RVD}	Delay from nIOR, IOR to Data		125	ns	100 pF loading
t_{WA}	Address Hold Time from nIOW, IOW	20		ns	Note 1
t_{WC}	Write Cycle Delay	150		ns	
t_{WCA}	Chip Select Hold Time from nIOW, IOW	20		ns	Note 1
t_{WR}	nIOW, IOW Strobe Width	100		ns	
t_{XH}	Duration of Clock High Pulse	55		ns	External Clock(8.0 MHz Max)
t_{XL}	Duration of Clock Low Pulse	55		ns	External Clock(8.0 MHz Max)
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$	280		ns	Note 4
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$	280		ns	

Baud Generator

N	Baud Divisor	1	$2^{16} - 1$		
t_{BHD}	Baud Output Positive Edge Delay		175	ns	100 pF load
t_{BLD}	Baud Output Negative Edge Delay		175	ns	100 pF load
t_{HW}	Baud Output Up Time	75		ns	$f_x = 8.0\text{MHz}$, $\div 2$, 100 pF load
t_{LW}	Baud Output Down Time	100		ns	$f_x = 8.0\text{MHz}$, $\div 2$, 100 pF load

Receiver

t_{RINT}	Delay from nIOR, IOR (RD RBR/ or RD LSR) to Reset interrupt		1	μs	100 pF load
t_{SCD}	Delay from RCLK to sample Time		2	μs	
t_{SINT}	Delay from Stop to Set Interrupt		1	RCLK Cycles	Note 2

Transmitter

Symbol	Parameter	Min	Max	Units	Conditions
t_{HR}	Delay from IOW, nIOW (WR THR) To Reset Interrupt		175	ns	100 pF load
t_{IR}	Delay from IOR, nIOR (RD IIR) To Reset Interrupt (THRE)		250	ns	100 pF load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	Baudout Cycles	
t_{SI}	Delay from Initial Write to Interrupt	16	24	Baudout Cycles	Note 5
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	Baudout Cycles	Note 5
t_{SXA}	Delay from Start to TXRDY active		8	Baudout Cycles	100 pF load
t_{WXI}	Delay from Write to TXRDY inactive		195	ns	100 pF load

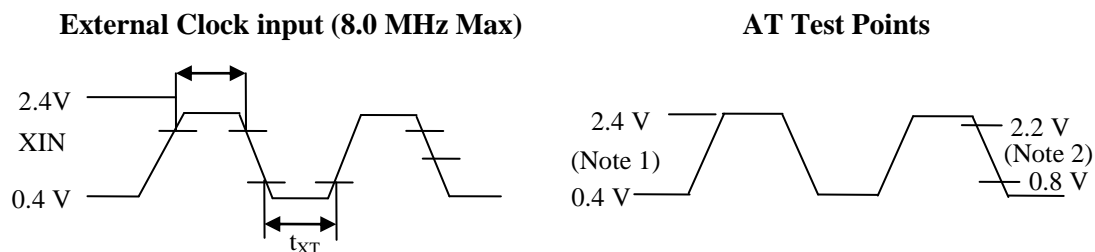
Modem Control

t_{MDO}	Delay from IOW, nIOW (WR MCR) to Output		200	ns	100 pF load
t_{RIM}	Delay to Reset Interrupt from IOR, nIOR (RD MSR)		250	ns	100 pF load
t_{SIM}	Delay to Set Interrupt from MIDEM Input		250	ns	100 pF load

Notes

1. Applicable only when nAS is tied low.
2. In the FIFO mode (FCR0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.
3. Charge and discharge time determined by V_{OL} , V_{OH} and the external loading.
4. In FIFO mode $RC = 425$ ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).
5. This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active (See FIFO interrupt Mode Operation)

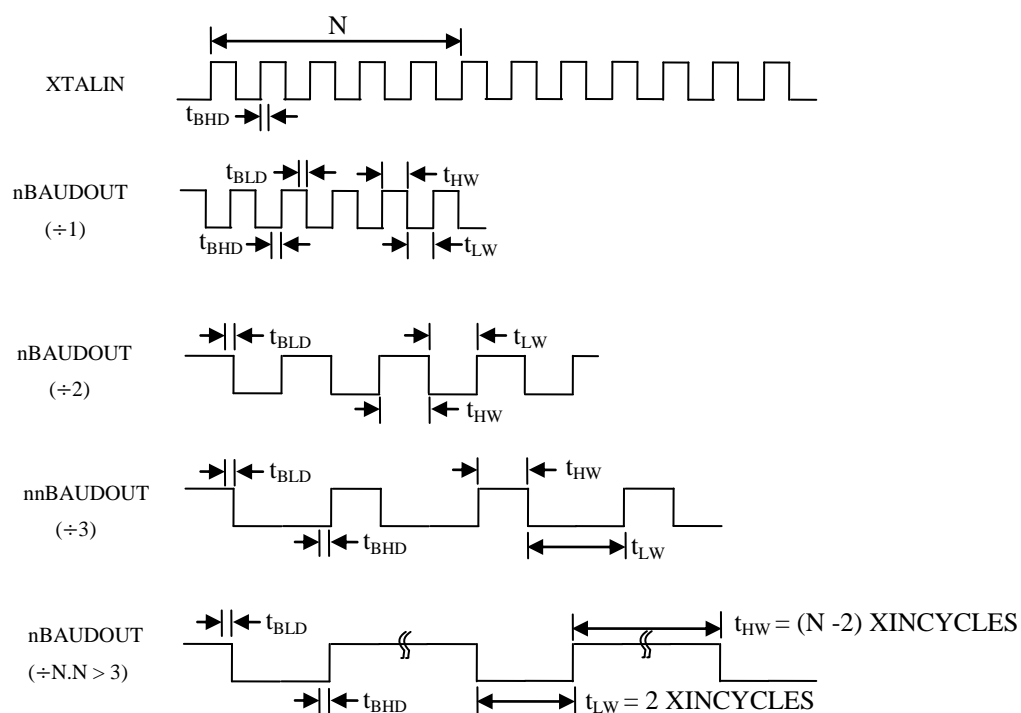
7. TIMING WAVEFORMS (All timings are referenced to valid 0 and valid 1)



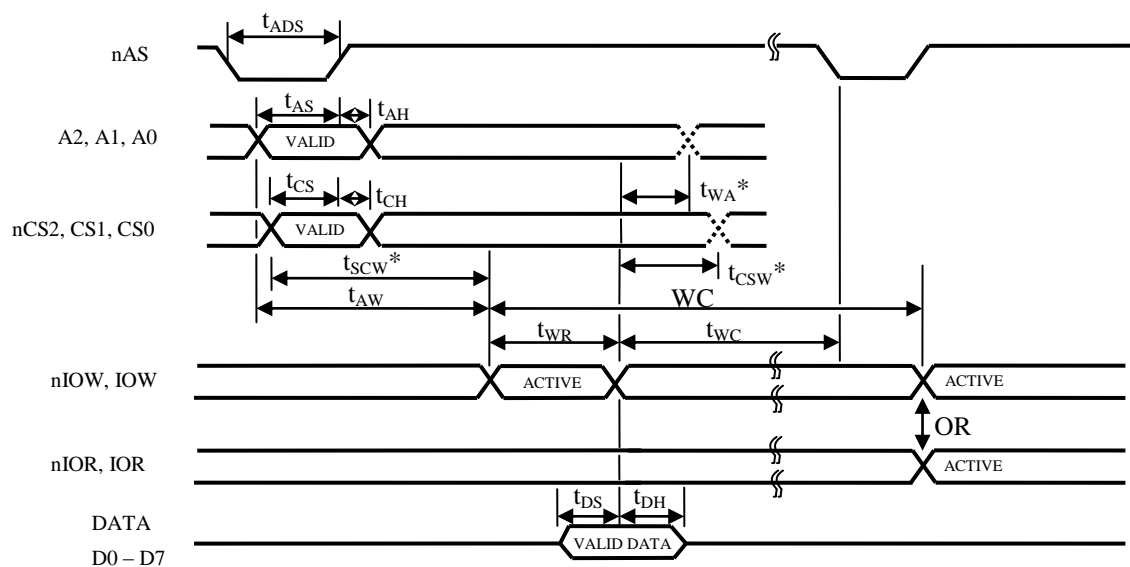
Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

Note 2: The 2.2V and 0.8V levels are the voltages at which the timing tests are made.

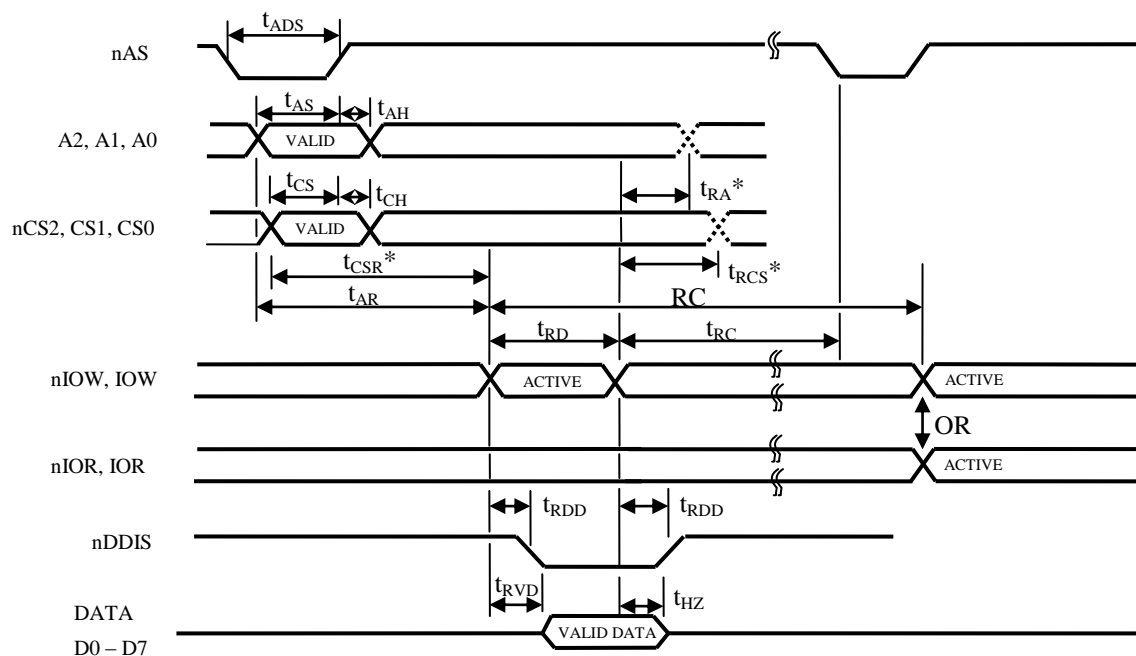
BAUDOUT Timing



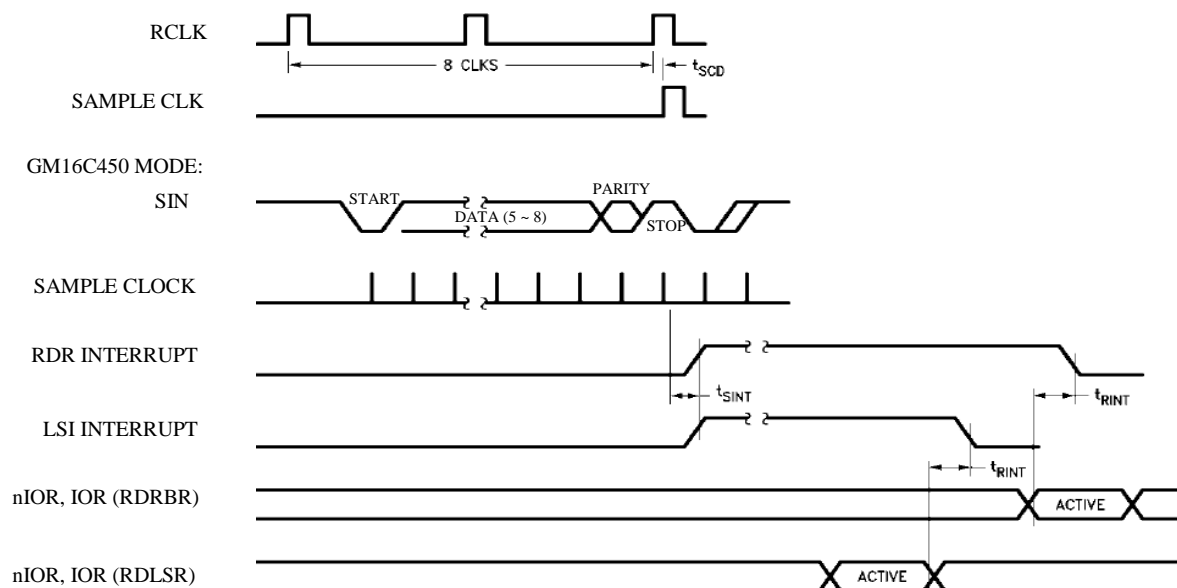
Write Cycle



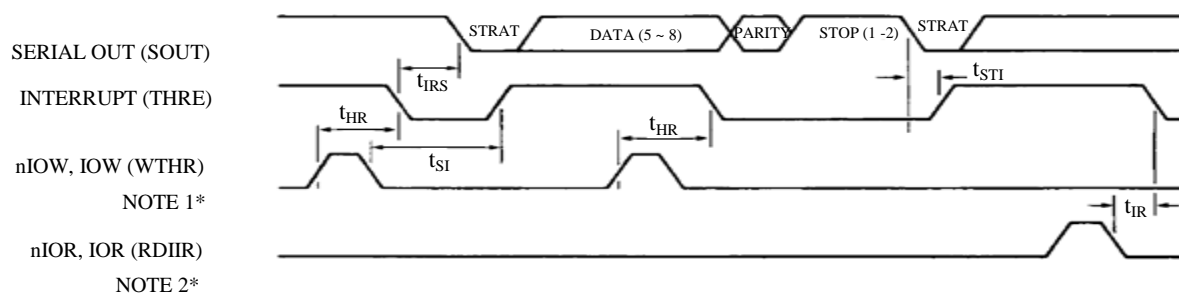
Read Cycle



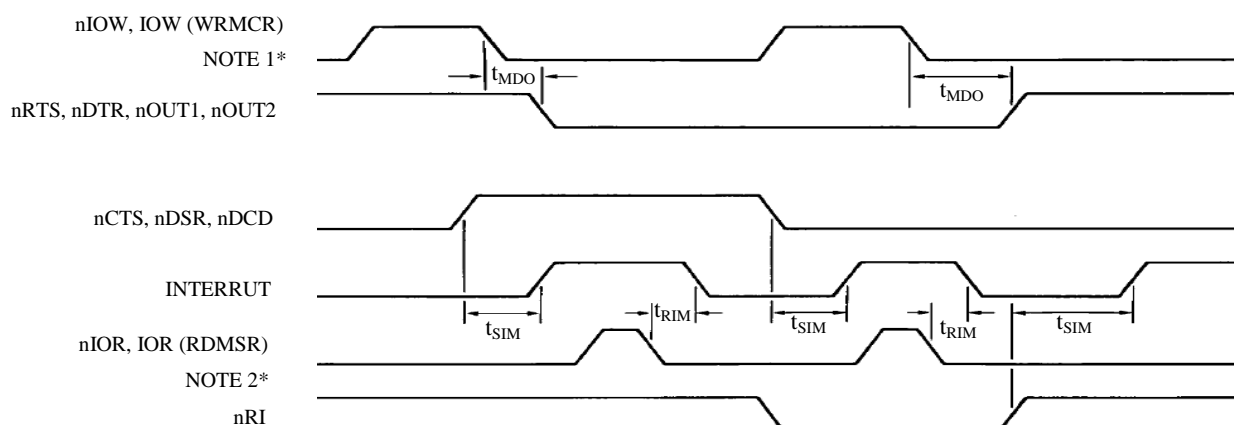
Receiver Timing



Transmitter Timing



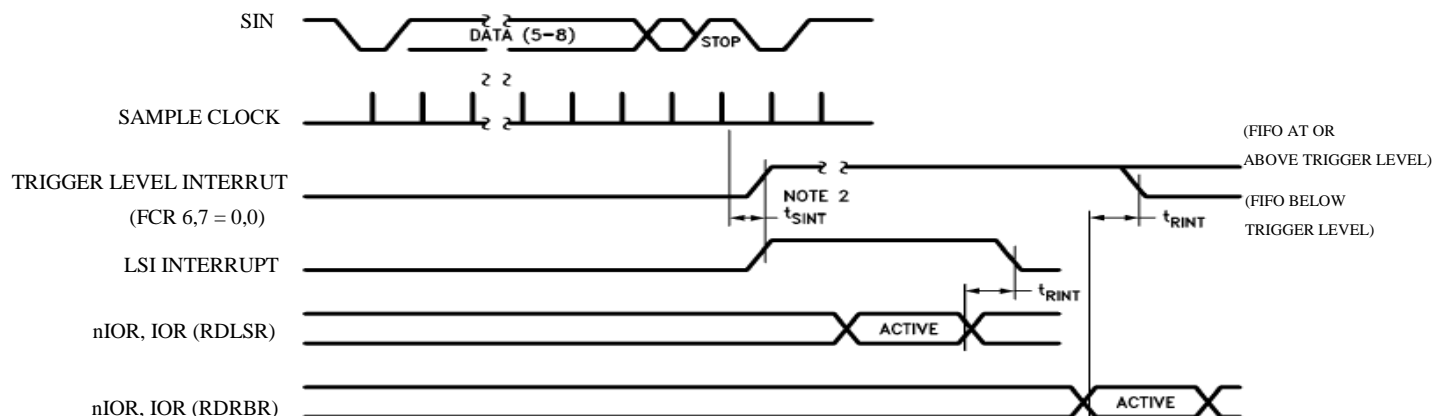
MODEM Control Timing



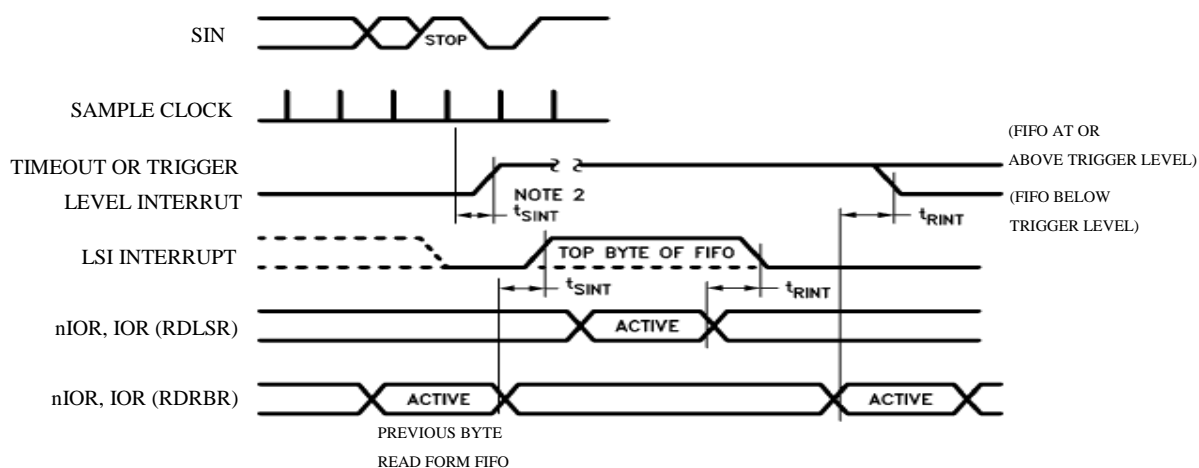
Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

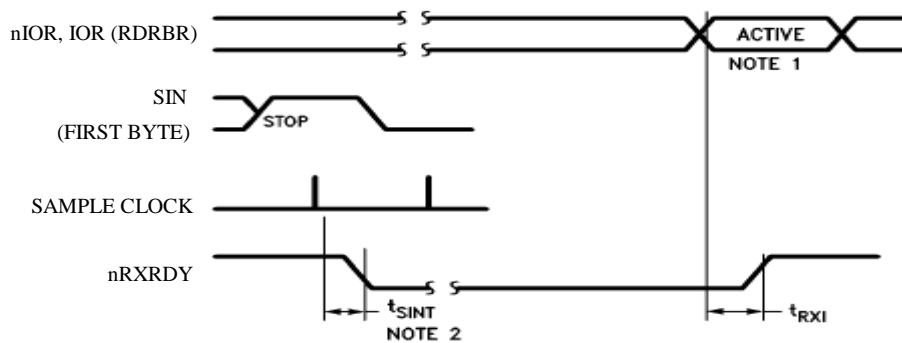
RCVR FIFO First Byte (This Sets RDR)



RCVR FIFO Bytes Other Than the First Byte (RDR Is Already Set)



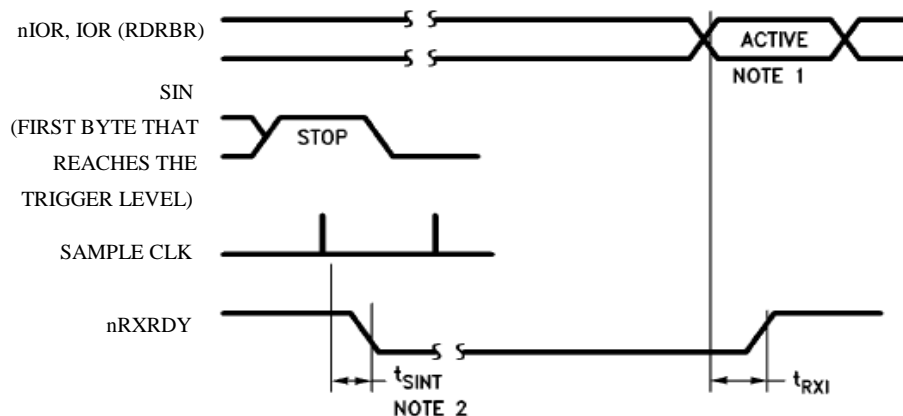
Receiver Ready FCR0=0 or FCR0=1 and FCR3=0 (Mode 0)



Note 1: This is the reading of the last byte in the FIFOs

Note 2: If FCR0 = 1, then $t_{SINT} = 3$ RCLKs. For a timeout interrupt, $t_{SINT} = 8$ RCLKs

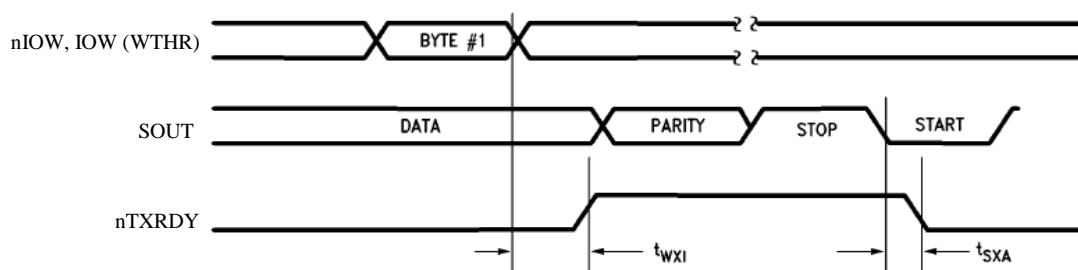
Receiver Ready FCR0 = 1 and FCR3 = 1 (Mode 1)



Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, $t_{SINT} = 3$ RCLKs.

Transmitter Ready FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



Transmitter Ready FCR0 = 1 and FCR3 = 1 (Mode 1)

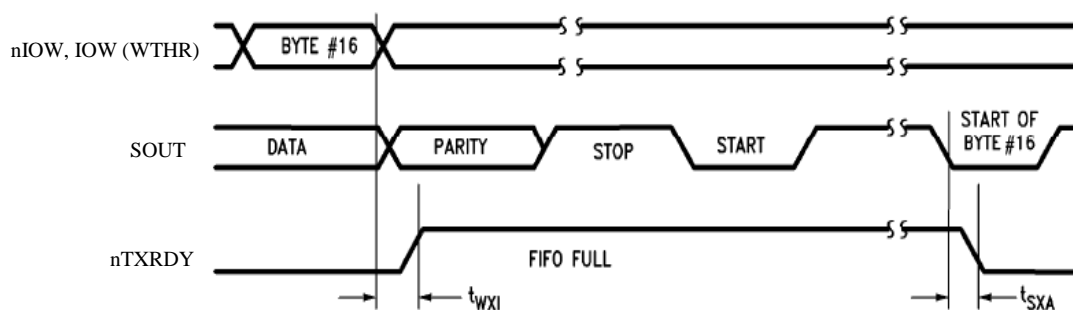


TABLE II. Summary of Registers

Bit No.	Register Address									
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register Ready (THRE)	Data Set Ready (DSR)	Bit 5
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: These bits are always 0 in the 16450 Mode.

8. REGISTERS

The system programmer may access any of the UART registers summarized in Table II via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table II has its name and reset state shown.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and set the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4

and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

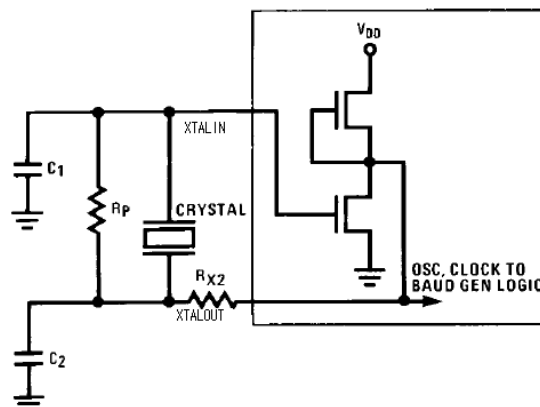
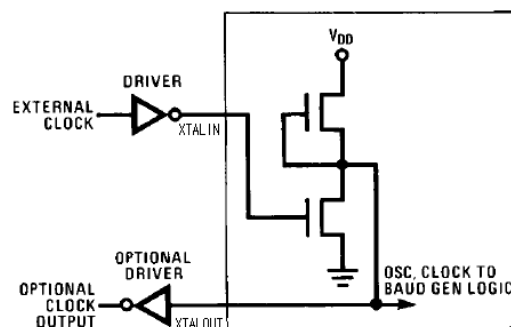
Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
 2. Set break after the next THRE.
 3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.
- During the break, the Transmitter can be used as a character timer to accurately establish the break duration..

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

8.2 TYPICAL CLOCK CIRCUITS



Typical Crystal Oscillator Network (Note)

CRYSTAL	R _p	R _{x2}	C ₁	C ₂
3.1MHz	1MΩ	1.5k	10-30 pF	40-60 pF
1.8MHz	1MΩ	1.5k	10-30 pF	40-60 pF

Note: These R and C values are approximate and may vary 2x depending on the crystal characteristics. All crystal circuits should be designed specifically for the system.

TABLE III. Baud Rates, Divisors and Crystals

Baud Rate	1.8432MHz Crystal		3.072MHz Crystal		8.0MHz Crystal	
	Decimal Divisor For 16Xclock	Percent Error	Decimal Divisor For 16Xclock	Percent Error	Decimal Divisor For 16Xclock	Percent Error
50	2304	-	3840	-	10000	-
75	1536	-	2560	-	6667	0.005
110	1047	0.026	1745	0.026	4545	0.010
134.5	857	0.058	1428	0.034	3717	0.013
150	768	-	1280	-	3333	0.010
300	384	-	640	-	1667	0.020
600	192	-	320	-	833	0.040
1200	96	-	160	-	417	0.080
1800	64	-	107	0.312	277	0.080
2000	58	0.69	96	-	250	-
2400	48	-	80	-	208	0.160
3600	32	-	53	0.628	139	0.080
4800	24	-	40	-	104	0.160
7200	16	-	27	1.23	69	0.644
9600	12	-	20	-	52	0.160
19200	6	-	10	-	26	0.160
38400	3	-	5	-	13	0.160
56000	2	2.86	-	-	9	0.790
128000	-	-	-	-	4	2.344
256000	-	-	-	-	2	2.344

8.3 PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 2 to $2^{16}-1$. The output frequency of the Baud Generator is $16 \times \frac{\text{Baud [divisor \#]} \times (\text{frequency input})}{(\text{frequency input}) \div (\text{baud rate} \times 16)}$. Two 8-bit latches store the divisor in a 16-bit binary format.

These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table III provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8.0 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

8.4 LINE STATUS REGISTER

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Details on each bit follow.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this

error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmitter Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

TABLE IV. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions				
	Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
	0	0	0	1	—	None	None	—
	0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
	0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
	1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 Char. Times and There Is at Least 1 Char. in It During This Time	Reading the Receiver Buffer Register
	0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
	0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 7: In the 16450 Mode this is a 0. In the FIFO mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the software must load a data byte in the Rx FIFO via Loopback Mode in order to write to LSR2-LSR4. LSR0 and LSR7 can't be written to in FIFO mode.

8.5 FIFO CONTROL REGISTER

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from the FIFO Mode to the 16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to

this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0=1 (see description of RXRDY and TXRDY pins).

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

		RCVR FIFO Trigger Level (Bytes)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

8.6 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table IV.

Bit 3: In the 16450 Mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: These two bits are set when FCR0=1.

8.7 INTERRUPT ENABLE REGISTER

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

8.8 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below.

Bit 0: This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic 1, the nDTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the nDTR output is forced to a logic 1.

Note: The nDTR output of the UART may be applied to an EIA inverting line driver to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (nOUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the nOUT 1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (nOUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the nOUT 2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (nDSR, nCTS, RI, and nDCD) are disconnected; and the four MODEM Control outputs (nDTR, nRTS, nOUT 1, and nOUT 2) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the UART. In the loopback mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.9 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the

MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the nCTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the nDSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the nRI input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (nCTS) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

8.10 SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

8.11 FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR0=1, IER0=1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.

D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (i.e., 1 Start, 8 Data, 1 Parity and 2 Stop Bits).

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0=1, IER1=1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

8.12 FIFO POLLED MODE OPERATION

With FCR0=1 resetting IER0, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation. In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the

same way as when in the interrupt mode, the IIR is not affected since IER2=0.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

9. TYPICAL APPLICATIONS

This shows the basic connections of an MC16C550 to an 8088 CPU

