FAIRCHILD SEMICONDUCTOR®

February 2009

FDD8447L_F085

N-Channel PowerTrench® MOSFET

40V, 50A, 11.0mΩ

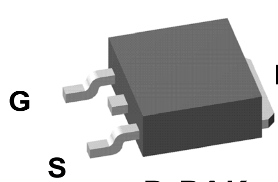
Features

- Typ $r_{DS(on)}$ = 7.0mΩ at V_{GS} = 10V, I_D = 14A
- Typ $r_{DS(on)}$ = 8.5mΩ at V_{GS} = 4.5V, I_D = 11A
- Fast Switching
- Qualified to AEC Q101
- RoHS Compliant

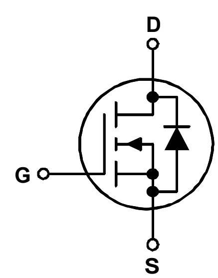
Applications

- Inverter
- Power Supplies
- Automotive Engine Control
- Power Train Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Primary Switch for 12V and 24V Systems

100% RoHS COMPLIANT



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage	(Note 1)	40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current Continuous (T_C < 80°C, V_{GS} = 10V)		50	A
	Pulsed		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	40	mJ
P_D	Power Dissipation		65	W
	Dreate above 25°C		0.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8447L	FDD8447L_F085	D-PAK(TO-252)	13”	12mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V	-	-	1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{GS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	1.0	1.9	3.0	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 14A, V_{GS} = 10V	-	7.0	8.5	mΩ
		I_D = 11A, V_{GS} = 4.5V	-	8.5	11.0	
		I_D = 14A, V_{GS} = 10V, T_J = 125°C	-	10.4	14.0	
g_{FS}	Forward Transconductance	I_D = 14A, V_{DS} = 5V	-	58	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	1970	-	pF
C_{oss}	Output Capacitance		-	250	-	pF
C_{rss}	Reverse Transfer Capacitance		-	150	-	pF
R_g	Gate Resistance	f = 1MHz	-	1.27	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V; V_{DD} = 20V, I_D = 14A, V_{GS} = 10V	-	37	52	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0 to 5V	-	20	28	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	7	-	nC

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	-	12	21	ns
t_r	Rise Time		-	12	21	ns
$t_{d(off)}$	Turn-Off Delay Time		-	38	61	ns
t_f	Fall Time		-	9	18	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 14A	-	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 14A, dI_{SD}/dt = 100A/µs	-	22	29	ns
Q_{rr}	Reverse Recovery Charge		-	11	14	nC

Notes:

1: Starting $T_J = 25^oC$ to 175^oC.

2: Starting $T_J = 25^oC$, L = 0.05mH, I_{AS} = 40A

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

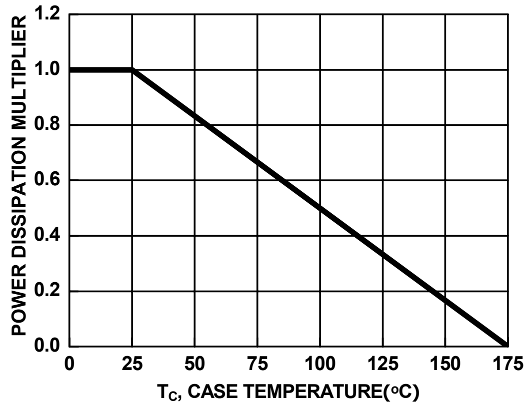


Figure 1. Normalized Power Dissipation vs Case Temperature

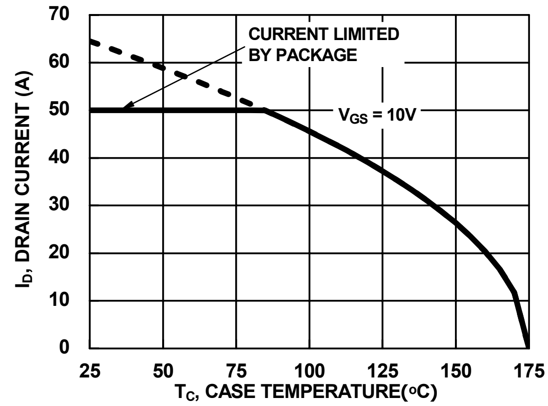


Figure 2. Maximum Continuous Drain Current vs Case Temperature

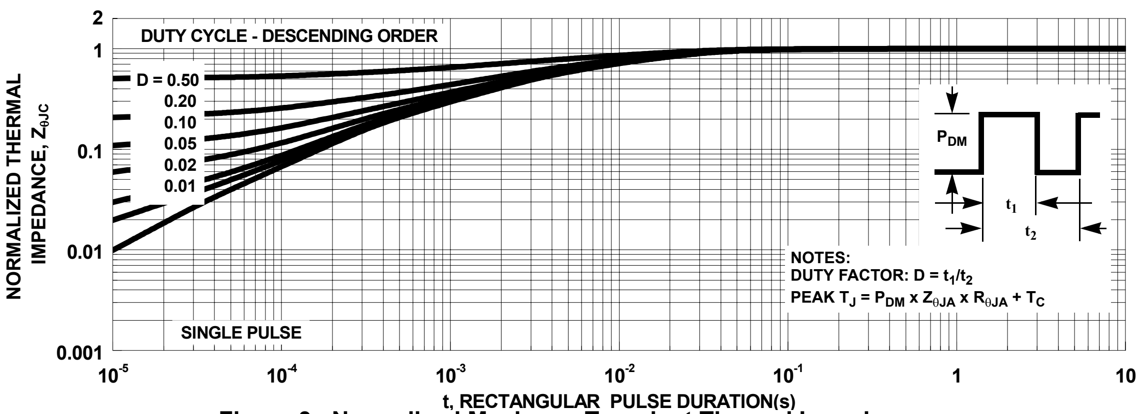


Figure 3. Normalized Maximum Transient Thermal Impedance

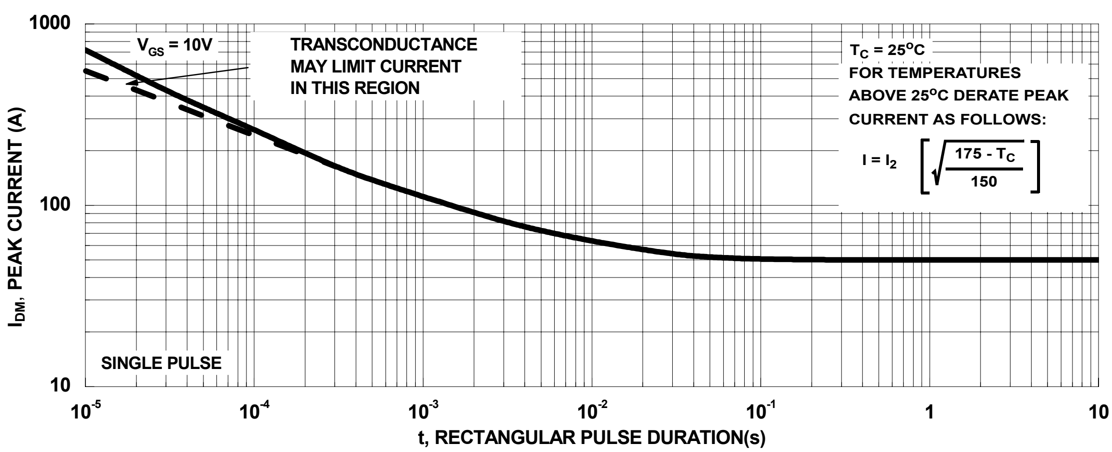


Figure 4. Peak Current Capability

Typical Characteristics

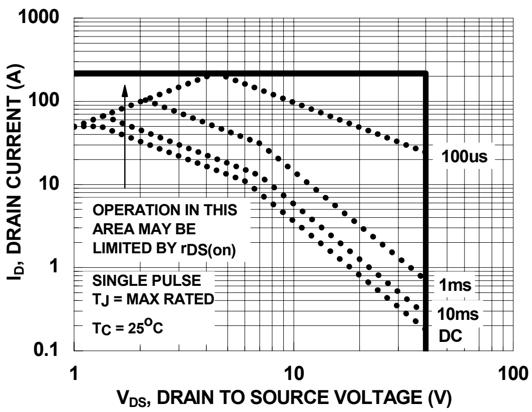
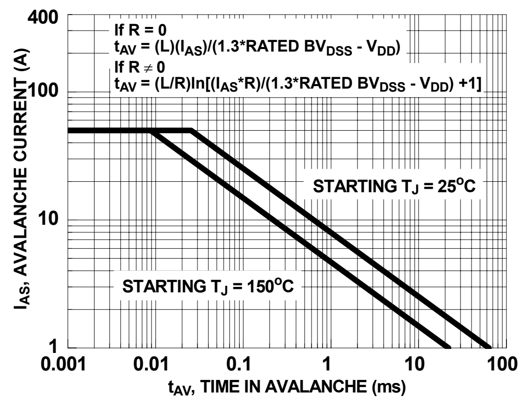


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

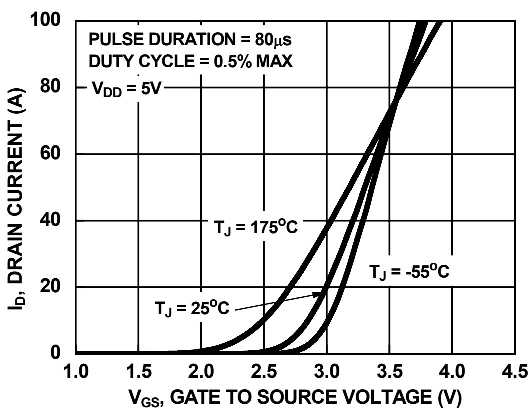


Figure 7. Transfer Characteristics

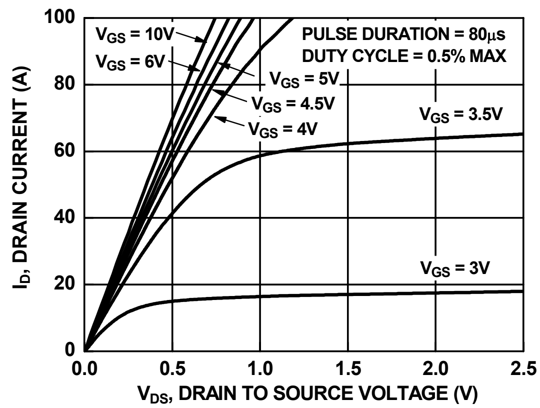


Figure 8. Saturation Characteristics

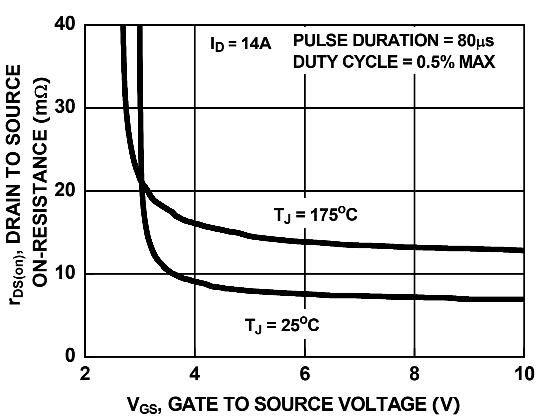


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

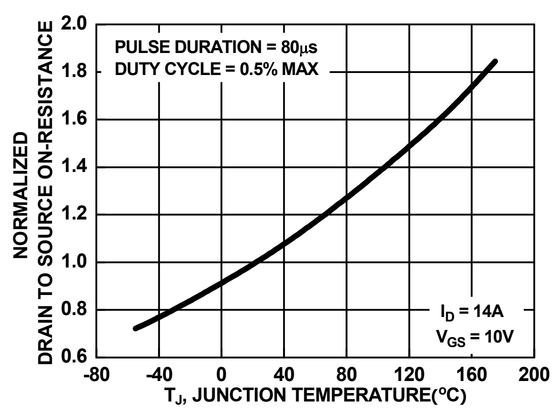


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

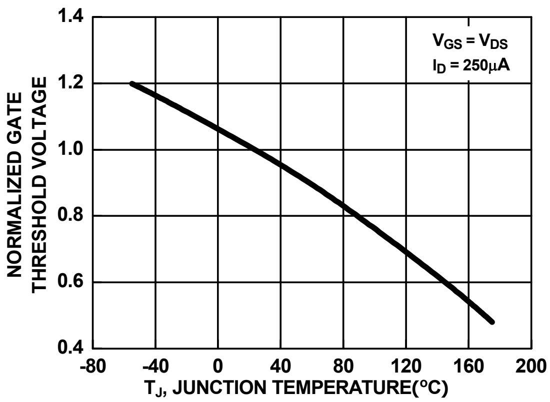


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

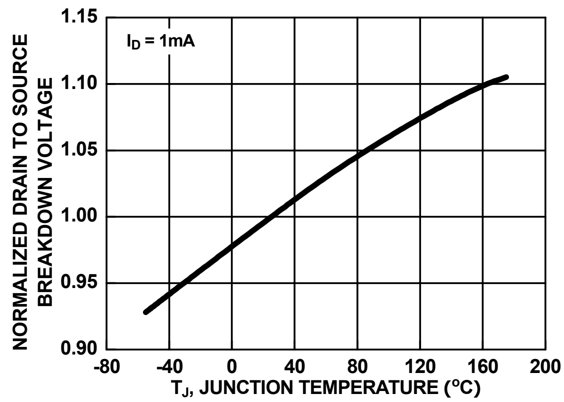


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

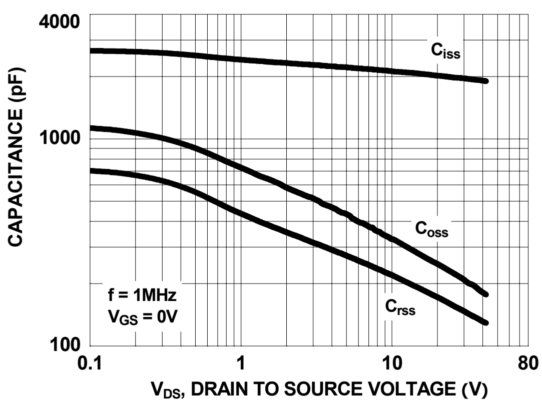


Figure 13. Capacitance vs Drain to Source Voltage

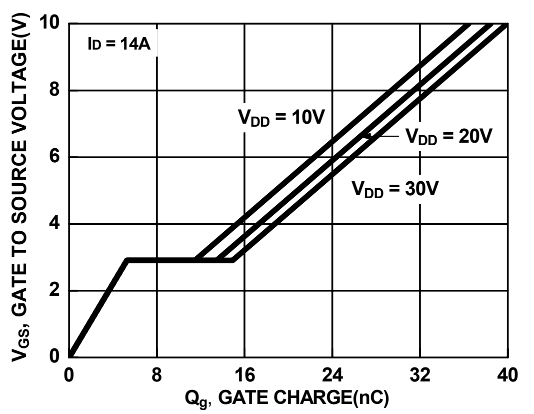


Figure 14. Gate Charge vs Gate to Source Voltage

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