

# MOS FIELD EFFECT TRANSISTOR

## 2SJ449

### SWITCHING P-CHANNEL MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SJ449 is P-Channel MOS Field Effect Transistor designed for high voltage switching applications.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)} = 0.8 \Omega \text{ MAX. (@ } V_{GS} = -10 \text{ V, } I_D = -3.0 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1040 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolated TO-220 Package

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

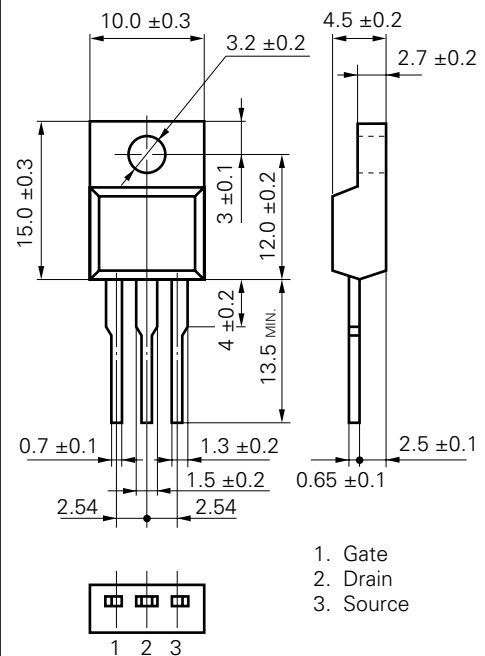
Drain to Source Voltage	$V_{DSS}$	-250	V
Gate to Source Voltage	$V_{GSS}$	$\mp 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 6.0$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\mp 24$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	-6.0	A
Single Avalanche Energy**	$E_{AS}$	180	mJ

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

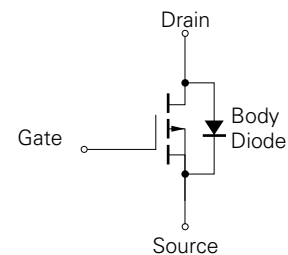
\*\* Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20 \text{ V} \rightarrow 0$

#### PACKAGE DIMENSIONS

(in millimeters)



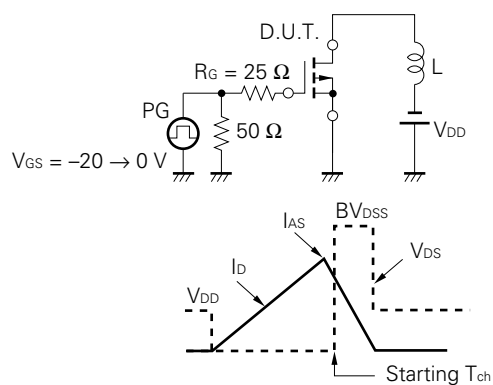
#### MP-45F (ISOLATED TO-220)



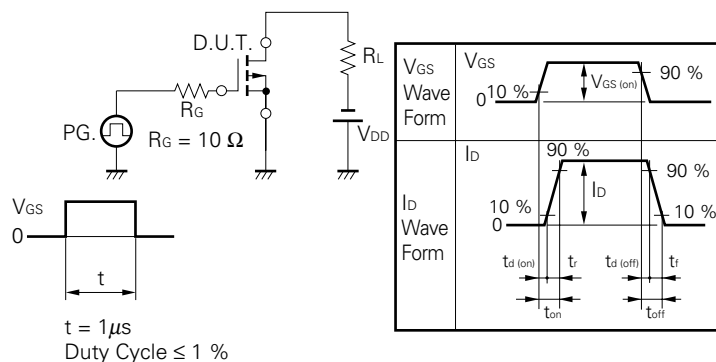
ELECTRICAL CHARACTERISTICS ( $T_A = 25\text{ }^{\circ}\text{C}$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS(on)}$		0.55	0.8	$\Omega$	$V_{GS} = -10\text{ V}$ , $I_D = -3.0\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-4.0	-4.8	-5.5	V	$V_{DS} = -10\text{ V}$ , $I_D = -1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	2.0	3.5		S	$V_{DS} = -10\text{ V}$ , $I_D = -3.0\text{ A}$
Drain Leakage Current	$I_{DSS}$			-100	$\mu\text{A}$	$V_{DS} = -250\text{ V}$ , $V_{GS} = 0$
Gate to Source Leakage Current	$I_{GSS}$			$\mp 100$	nA	$V_{GS} = \mp 30\text{ V}$ , $V_{DS} = 0$
Input Capacitance	$C_{iss}$		1040		pF	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	$C_{oss}$		360		pF	
Reverse Transfer Capacitance	$C_{rss}$		70		pF	
Turn-On Delay Time	$t_{d(on)}$		24		ns	
Rise Time	$t_r$		16		ns	$I_D = -3.0\text{ A}$ $V_{GS(on)} = -10\text{ V}$ $V_{DD} = -125\text{ V}$ $R_G = 10\text{ }\Omega$ , $R_L = 42\text{ }\Omega$
Turn-Off Delay Time	$t_{d(off)}$		47		ns	
Fall Time	$t_f$		14		ns	
Total Gate Charge	$Q_G$		23.1		nC	$I_D = -6.0\text{ A}$ $V_{DD} = -200\text{ V}$ $V_{GS} = -10\text{ V}$
Gate to Source Charge	$Q_{GS}$		7.1		nC	
Gate to Drain Charge	$Q_{GD}$		12.9		nC	
Body Diode Forward Voltage	$V_{F(S-D)}$		0.92		V	$I_F = -6.0\text{ A}$ , $V_{GS} = 0$
Reverse Recovery Time	$t_{rr}$		155		ns	$I_F = -6.0\text{ A}$ , $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{rr}$		930		nC	

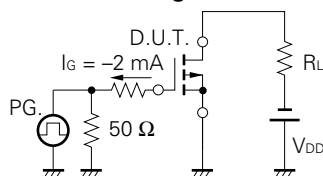
Test Circuit 1 Avalanche Capability



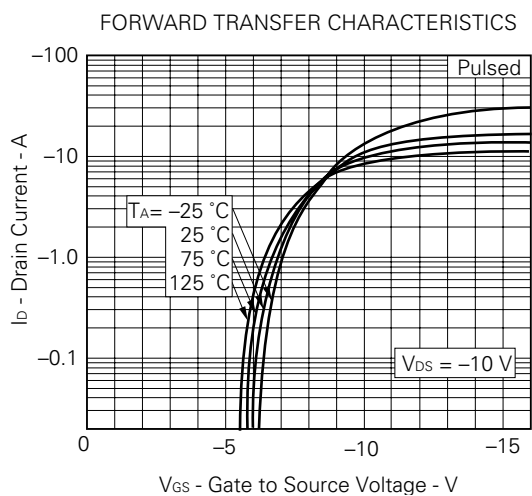
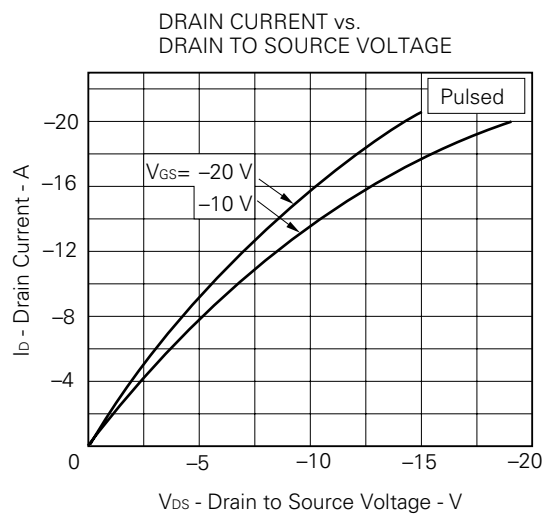
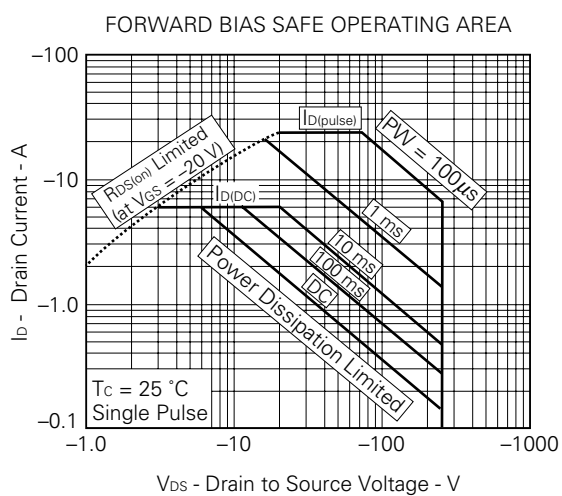
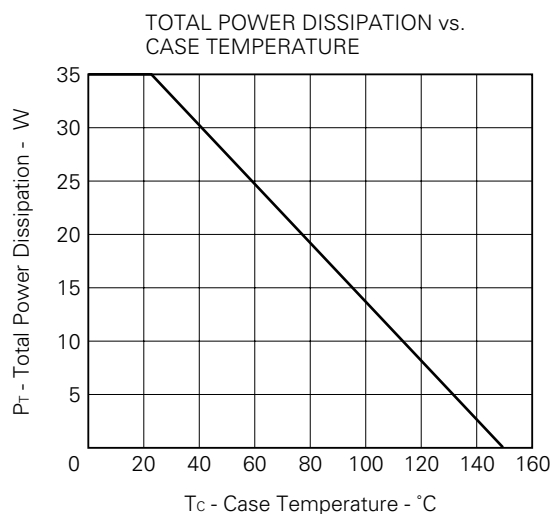
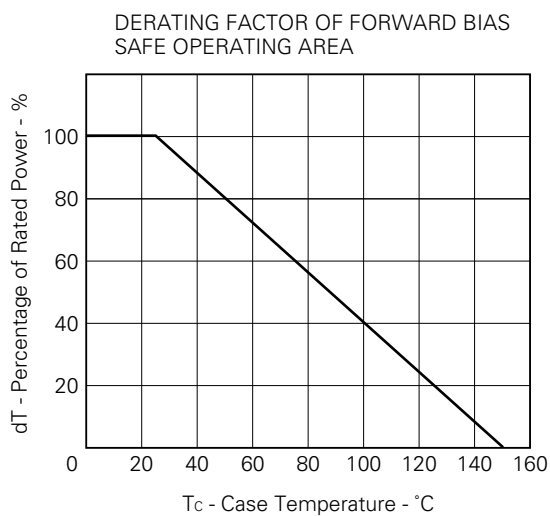
Test Circuit 2 Switching Time



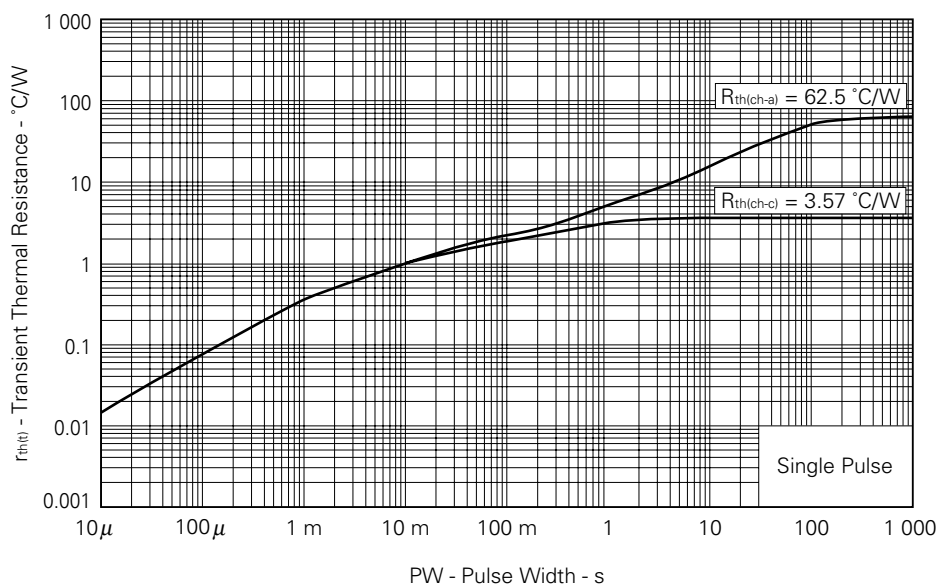
Test Circuit 3 Gate Charge



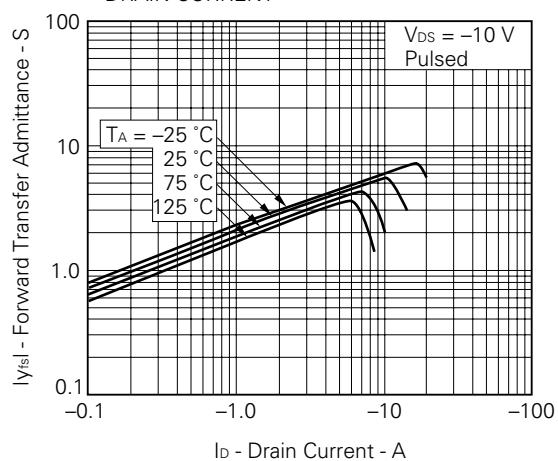
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS ( $T_A = 25\text{ }^{\circ}\text{C}$ )

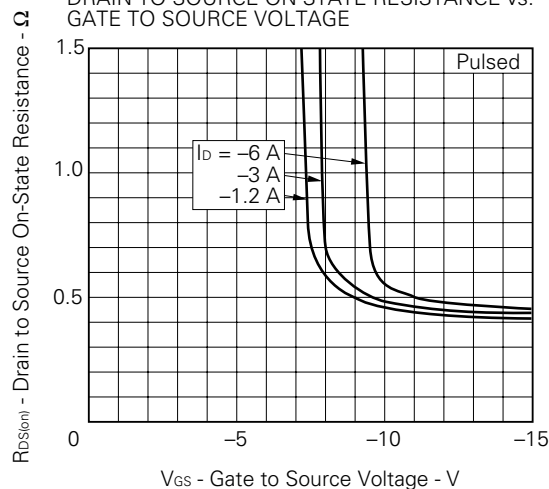
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



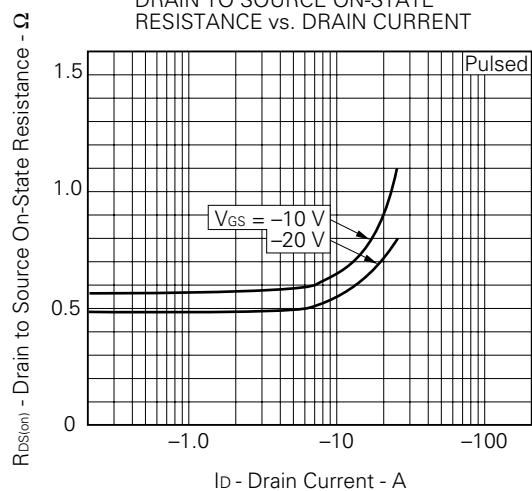
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



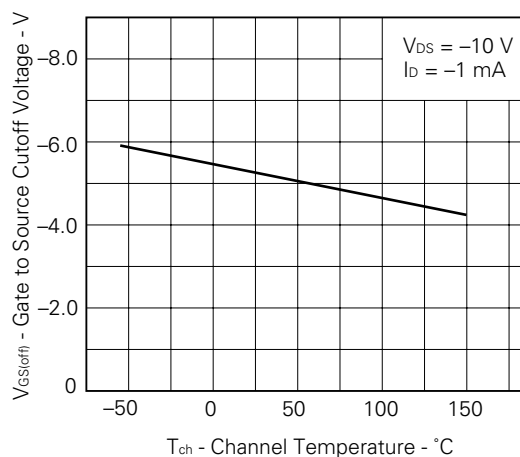
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



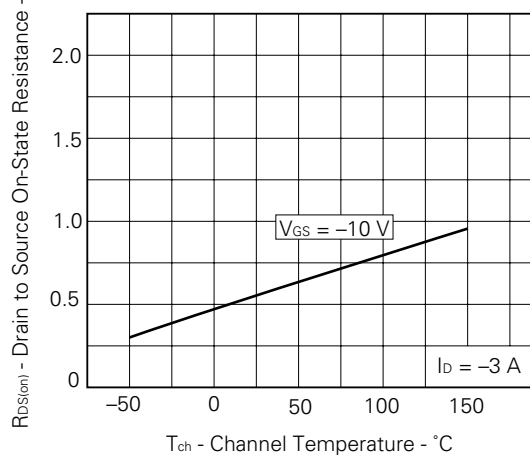
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



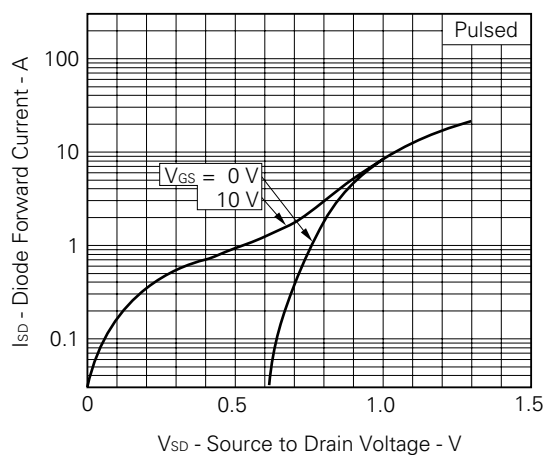
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



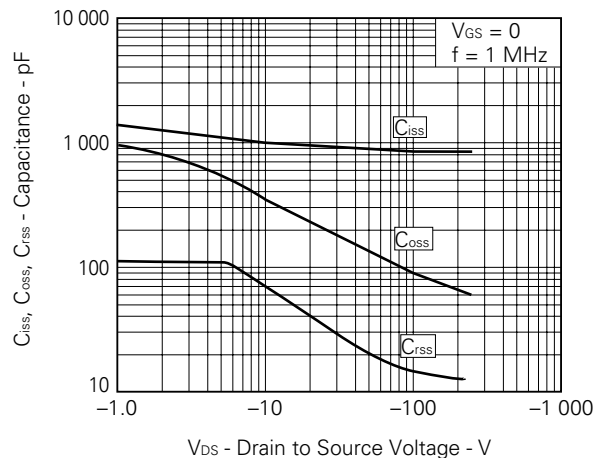
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



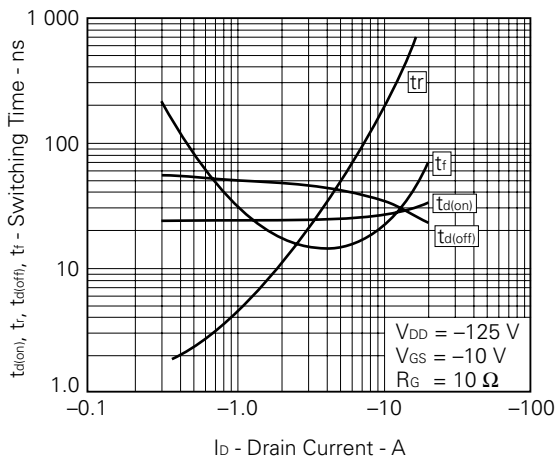
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



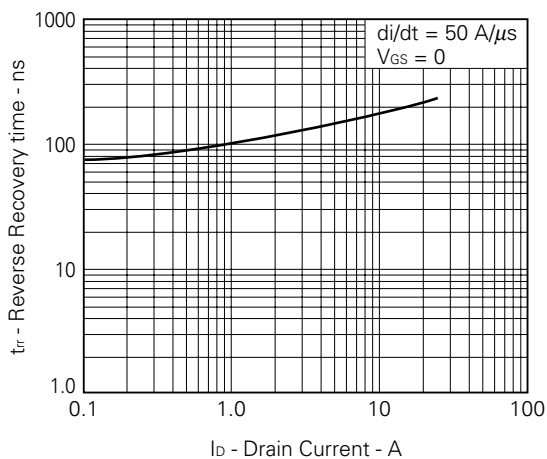
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



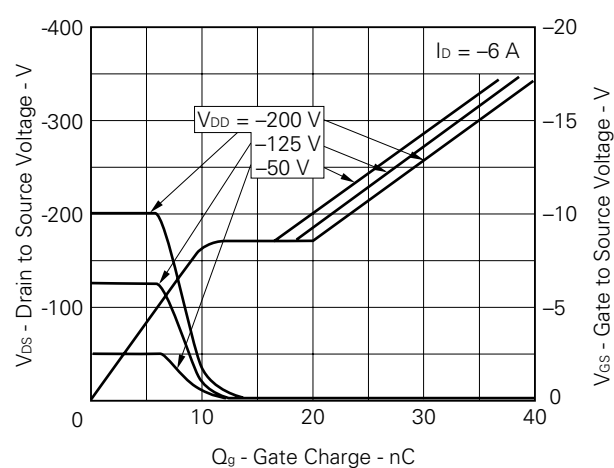
SWITCHING CHARACTERISTICS

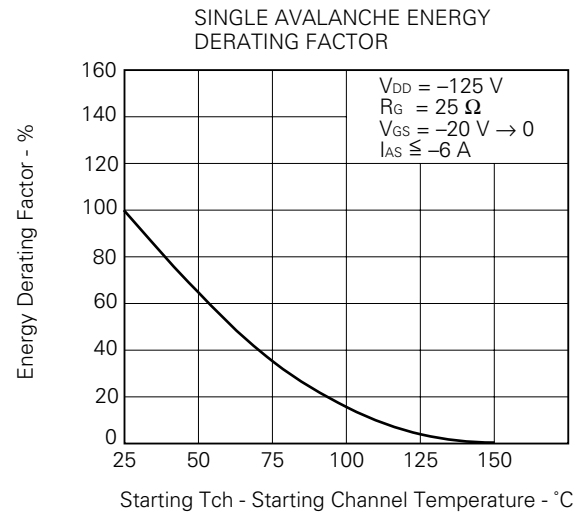
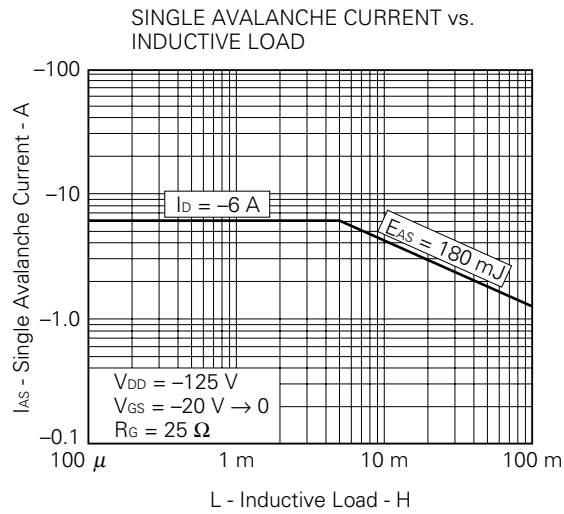


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS





## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.