DATA SHEET

MOS FIELD EFFECT TRANSISTOR

2SK2275

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2275 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 2.8 Ω MAX. (V_{GS} = 10 V, I_D = 2.0 A)
- Low C_{iss} C_{iss} = 1 000 pF TYP.
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D (DC)}$	±3.5	A
Drain Current (pulse)	$I_{D (pulse)}$*	±14	A
Total Power Dissipation (T_C = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Storage Temperature	T_{stg}	–55 to +150	°C
Channel Temperature	T_{ch}	150	°C
Single Avalanche Current	I_{AS}**	3.5	A
Single Avalanche Energy	E_{AS}**	22	mJ

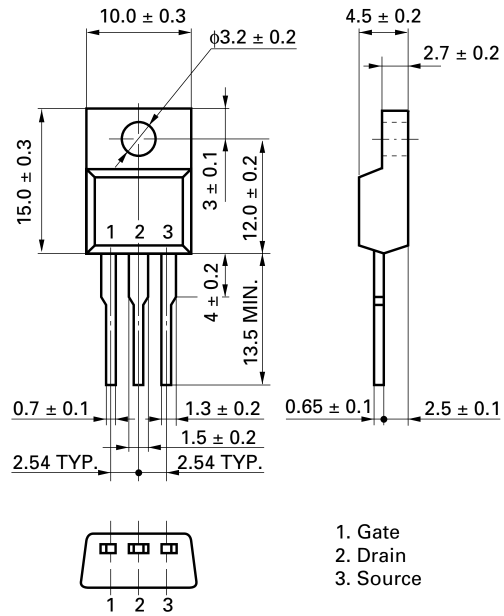
*PW ≤ 10 μs, Duty Cycle ≤ 1%

**Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

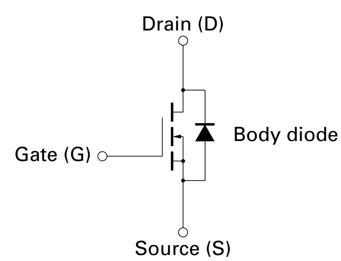
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DIMENSIONS

(in millimeters)



MP-45F (ISOLATED TO-220)



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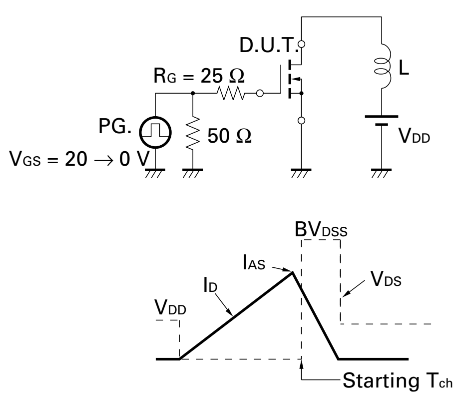
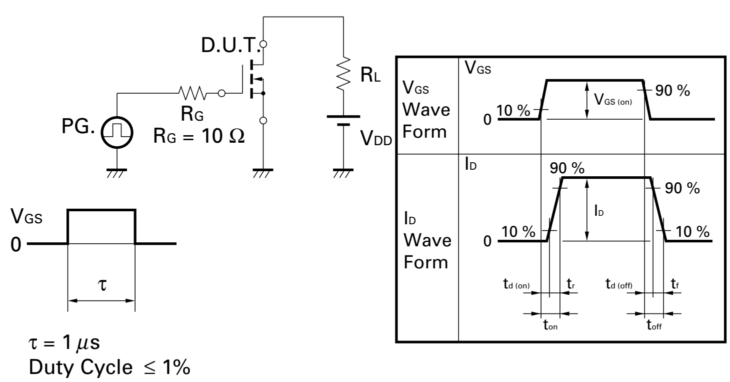
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		2.2	2.8	Ω	V_{GS} = 10 V, I_D = 2 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	1.0			S	V_{DS} = 20 V, I_D = 2 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 900 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1 000		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		170		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		60		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		20		ns	V_{GS} = 10 V
Rise Time	t_r		20		ns	V_{DD} = 150 V
Turn-Off Delay Time	$t_{d(off)}$		90		ns	I_D = 2 A, R_G = 10 Ω
Fall Time	t_f		20		ns	R_L = 75 Ω
Total Gate Charge	Q_G		42		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		6.0		nC	I_D = 3.5 A
Gate to Drain Charge	Q_{GD}		20		nC	V_{DD} = 450 V
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	I_F = 3.5 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		480		ns	1_F = 3.5 A
Reverse Recovery Charge	Q_{rr}		2.5		μC	di/dt = 50 A/μs

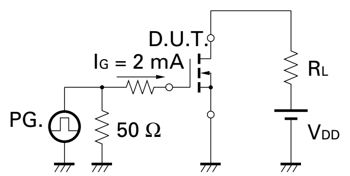
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time



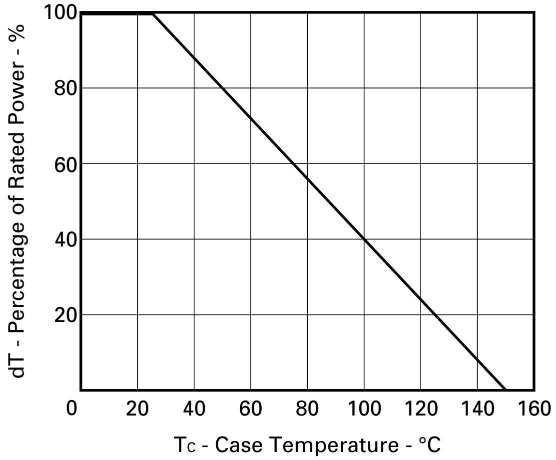
Test Circuit 3: Gate Charge



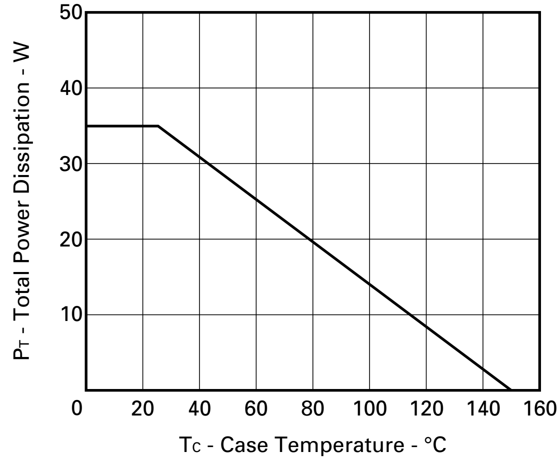
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (T_A = 25 °C)

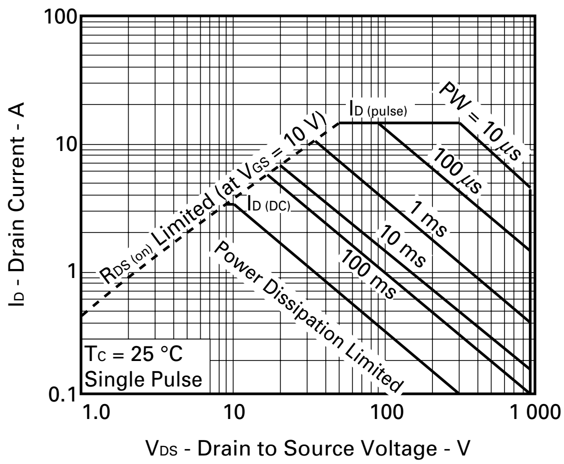
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



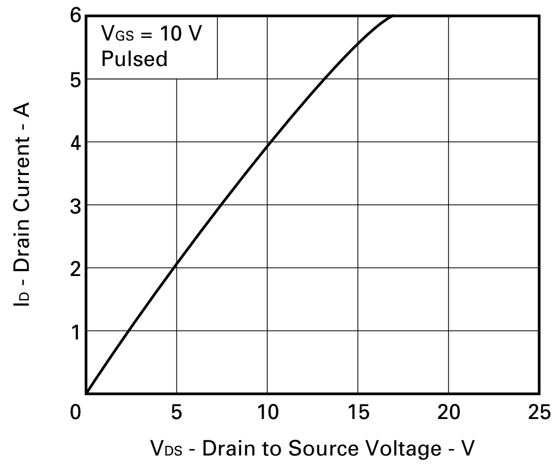
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



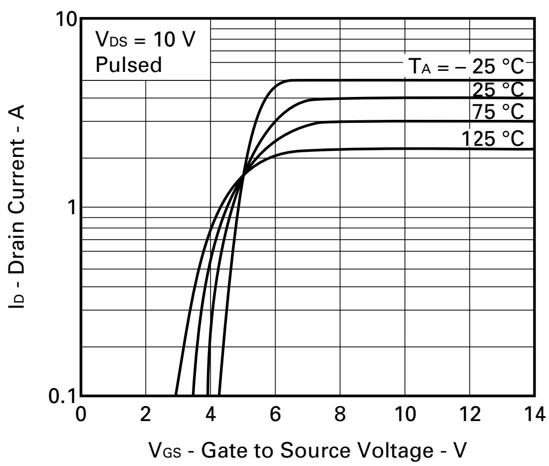
FORWARD BIAS SAFE OPERATING AREA

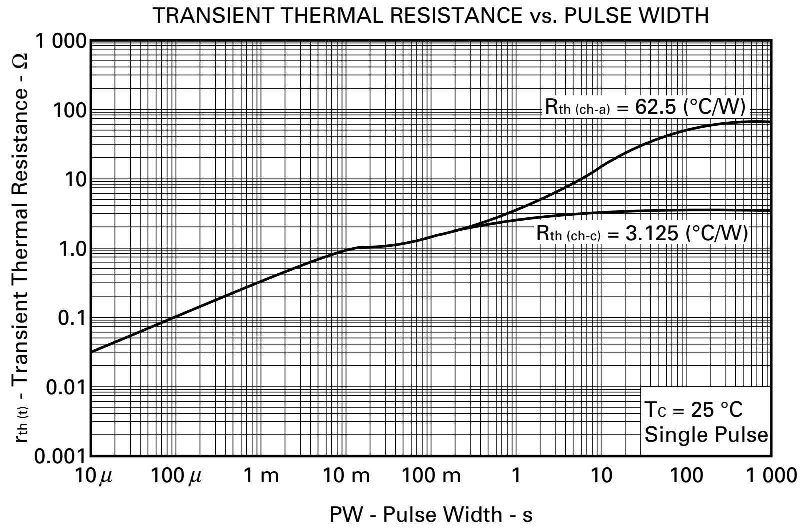


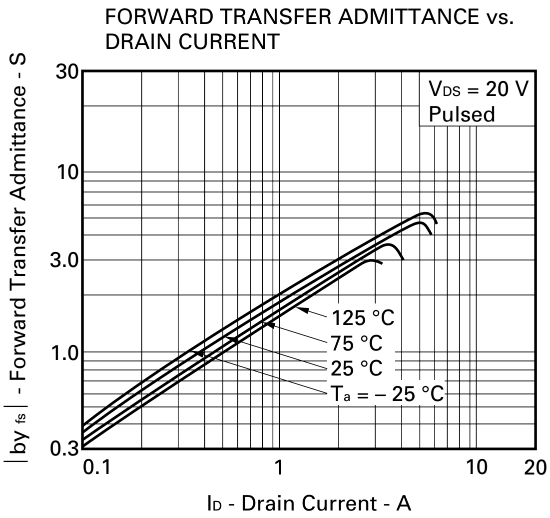
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

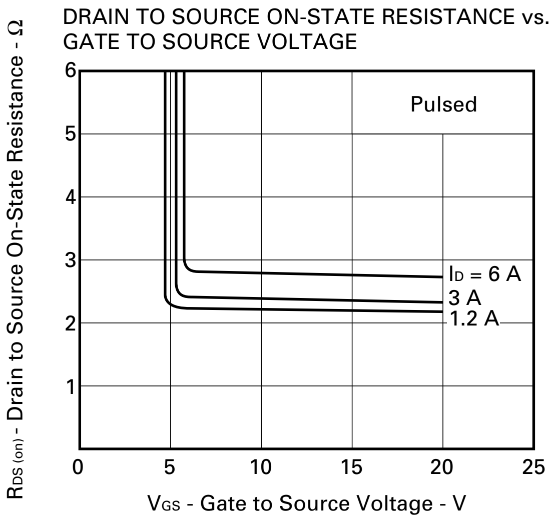


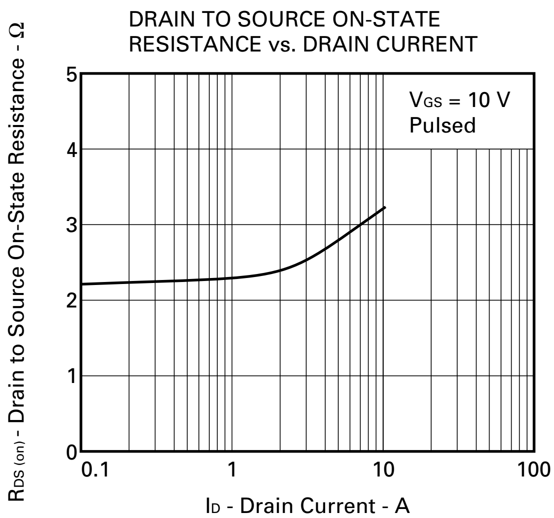
TRANSFER CHARACTERISTICS

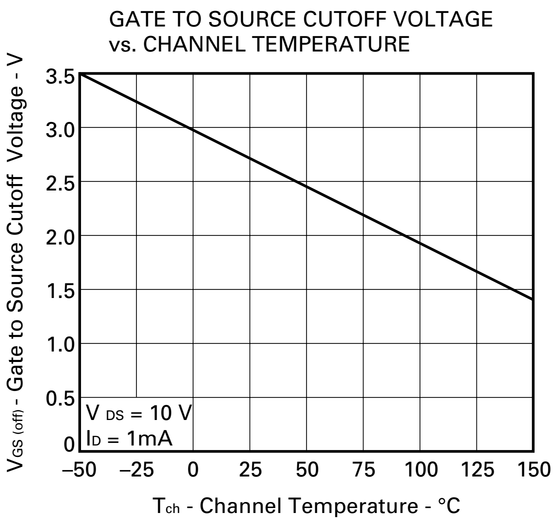



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
rth (t) - Transient Thermal Resistance - Ω
1 000
100
10
1.0
0.1
0.01
0.001
Rth (ch-a) = 62.5 (°C/W)
Rth (ch-c) = 3.125 (°C/W)
TC = 25 °C
Single Pulse
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1 000
PW - Pulse Width - s

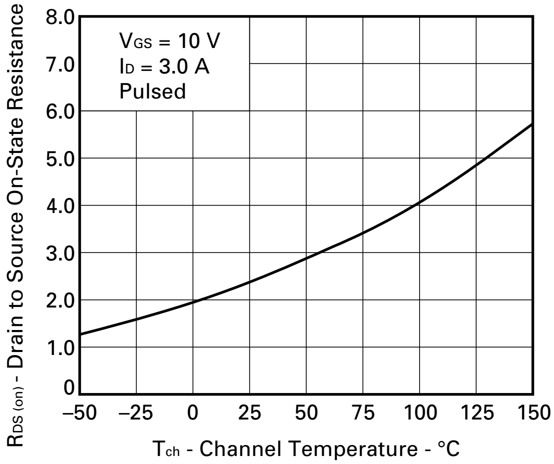

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT
|yfs| - Forward Transfer Admittance - S
30
10
3.0
1.0
0.3
VDS = 20 V
Pulsed
125 °C
75 °C
25 °C
Ta = – 25 °C
0.1
1
10
20
ID - Drain Current - A


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE
RDS (on) - Drain to Source On-State Resistance - Ω
6
5
4
3
2
1
Pulsed
ID = 6 A
3 A
1.2 A
0
5
10
15
20
25
VGS - Gate to Source Voltage - V

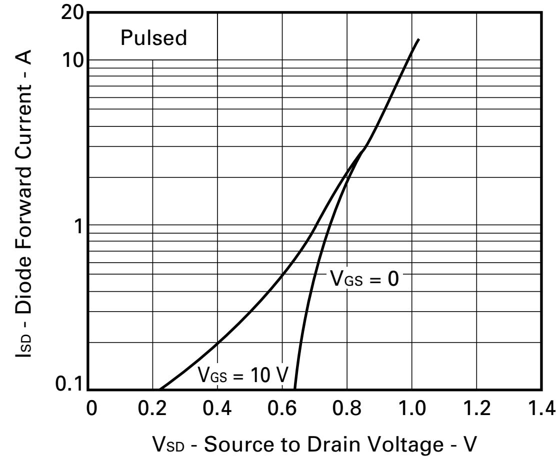

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT
RDS (on) - Drain to Source On-State Resistance - Ω
5
4
3
2
1
0
VGS = 10 V
Pulsed
0.1
1
10
100
ID - Drain Current - A


GATE TO SOURCE CUTOFF VOLTAGE
vs. CHANNEL TEMPERATURE
VGS (off) - Gate to Source Cutoff Voltage - V
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
V DS = 10 V
ID = 1mA
–50
–25
0
25
50
75
100
125
150
Tch - Channel Temperature - °C

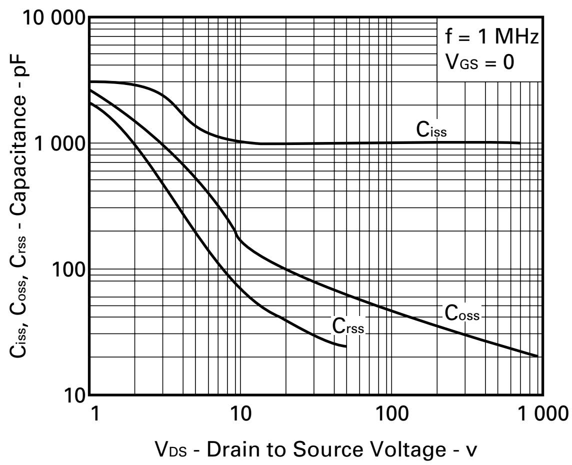
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



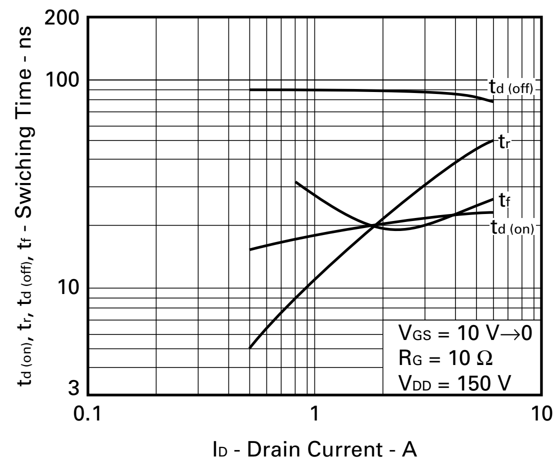
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



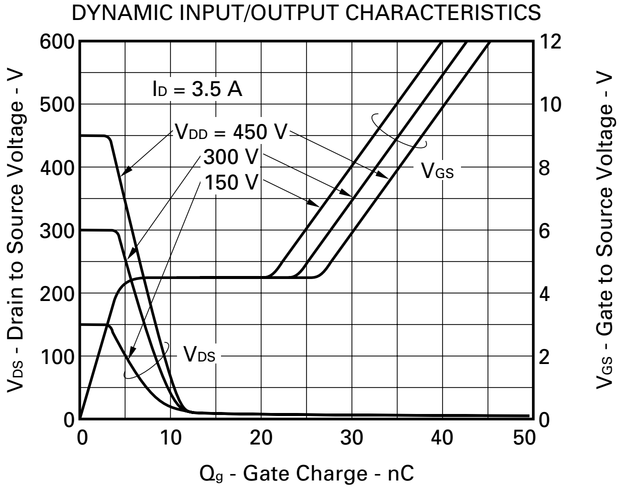
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



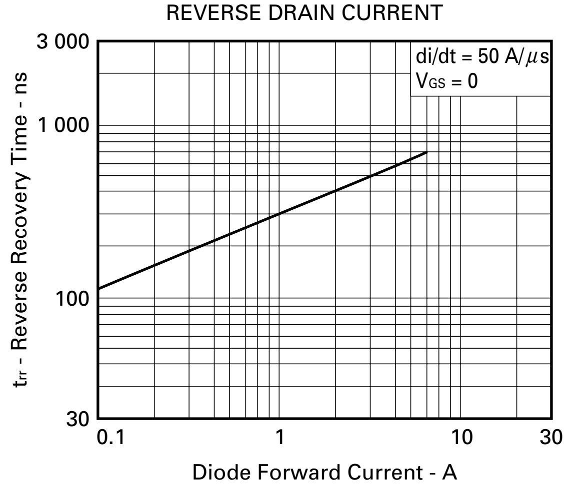
SWITCHING CHARACTERISTICS



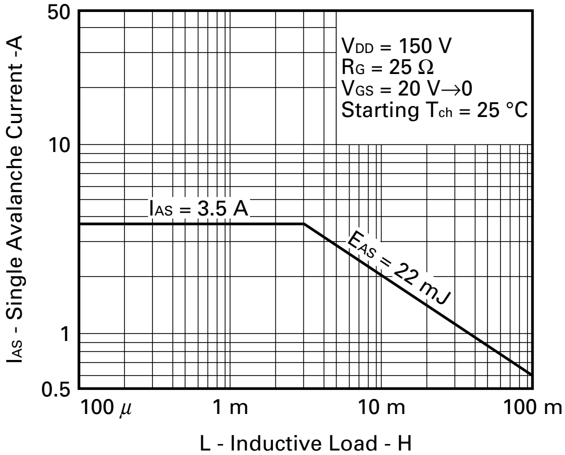
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



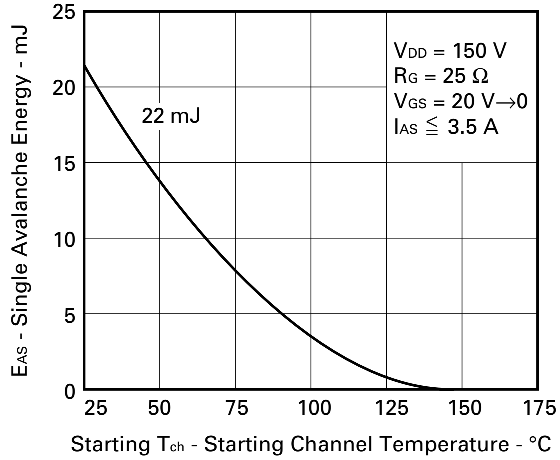
REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

[MEMO]