74HC283

4-bit binary full adder with fast carry

Rev. 03 — 11 November 2004 **Product data sheet**

1. General description

The 74HC283 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC283 is specified in compliance with JEDEC standard no. 7A.

The 74HC283 adds two 4-bit binary words (An plus Bn) plus the incoming carry (CIN). The binary sum appears on the sum outputs (S1 to S4) and the out-going carry (COUT) according to the equation:

CIN + (A1 + B1) + 2(A2 + B2) + 4(A3 + B3) + 8(A4 + B4) =
= S1 + 2S2 + 4S3 + 8S4 + 16COUT

Where (+) = plus.

Due to the symmetry of the binary add function, the 74HC283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic). In case of all active LOW operands the results S1 to S4 and COUT should be interpreted also as active LOW. With active HIGH inputs, CIN must be held LOW when no carry in is intended. Interchanging inputs of equal weight does not affect the operation, thus CIN, A1, B1 can be assigned arbitrarily to pins 5, 6, 7, etc.

See the 74HC583 for the BCD version.

2. Features

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V					
	CIN to S1			-	16	-	ns
	CIN to S2			-	18	-	ns
	CIN to S3			-	20	-	ns
	CIN to S4			-	23	-	ns
	An or Bn to Sn			-	21	-	ns
	CIN to COUT			-	20	-	ns
	An or Bn to COUT			-	20	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	88	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC283N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC283D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC283DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC283PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

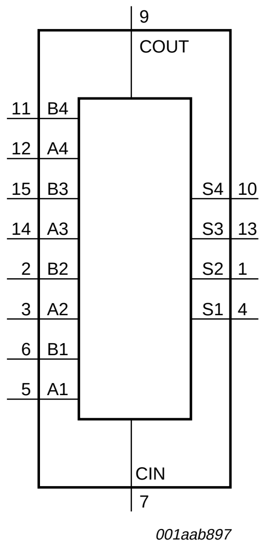


Fig 1. Functional diagram

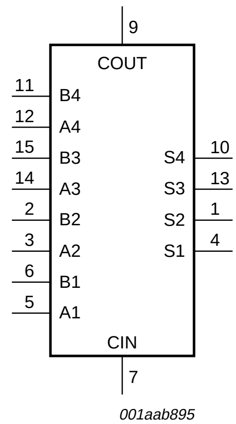


Fig 2. Logic symbol

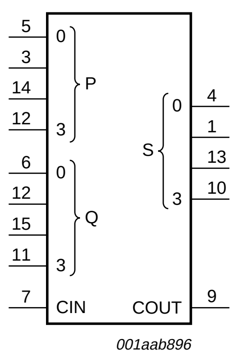


Fig 3. IEC logic symbol

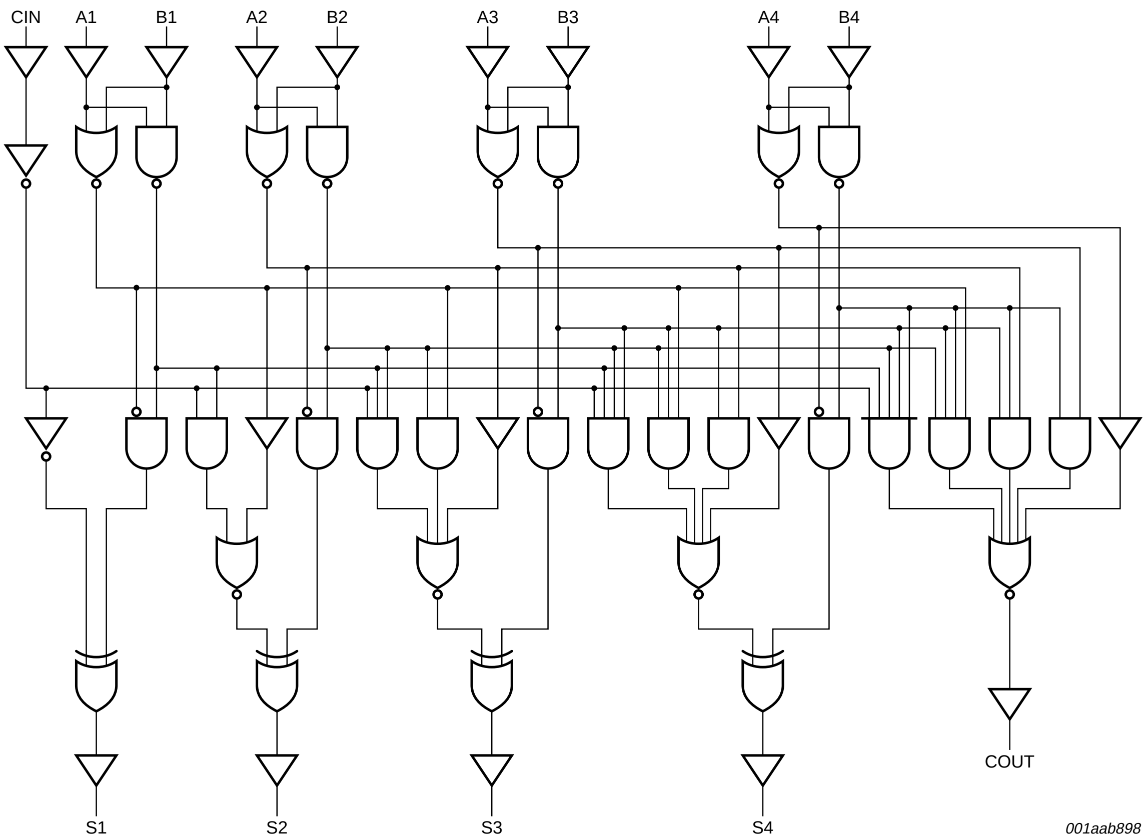


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

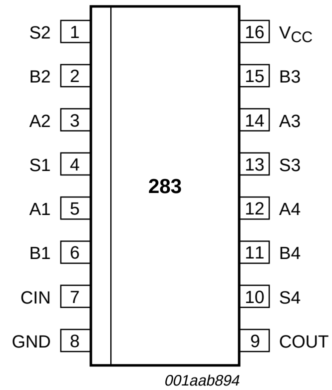


Fig 5. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
S2	1	sum output 2
B2	2	B operand input 2
A2	3	A operand input 2
S1	4	sum output 1
A1	5	A operand input 1
B1	6	B operand input 1
CIN	7	carry input
GND	8	ground (0 V)
COUT	9	carry output
S4	10	sum output 4
B4	11	B operand input 4
A4	12	A operand input 4
S3	13	sum output 3
B3	14	A operand input 3
A3	15	B operand input 3
V_{CC}	16	positive supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Pins	Input									Output				
	CIN	A4	A3	A2	A1	B4	B3	B2	B1	COUT	S4	S3	S2	S1
Logic levels	L	H	L	H	L	H	L	L	H	H	L	L	H	H
Active HIGH [2]	0	1	0	1	0	1	0	0	1	1	0	0	1	1
Active LOW [3]	1	0	1	0	1	0	1	1	0	0	1	1	0	0

[1] H = HIGH voltage level;
L = LOW voltage level.

[2] Example for active HIGH: 10 + 9 (0 + 1010 + 1001) = 19 (10011).

[3] Example for active LOW: 5 + 6 (1 + 0101 + 0110) = 12 (01100).

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16, SSOP16 and TSSOP16 packages		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CIN to S1	see Figure 6				
		V_{CC} = 2.0 V	-	52	160	ns
		V_{CC} = 4.5 V	-	19	32	ns
		V_{CC} = 6.0 V	-	15	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	ns
	propagation delay CIN to S2	see Figure 6				
		V_{CC} = 2.0 V	-	58	180	ns
		V_{CC} = 4.5 V	-	21	36	ns
		V_{CC} = 6.0 V	-	17	31	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	18	-	ns
	propagation delay CIN to S3	see Figure 6				
		V_{CC} = 2.0 V	-	63	195	ns
		V_{CC} = 4.5 V	-	23	39	ns
		V_{CC} = 6.0 V	-	18	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	ns
	propagation delay CIN to S4	see Figure 6				
		V_{CC} = 2.0 V	-	74	230	ns
		V_{CC} = 4.5 V	-	27	46	ns
		V_{CC} = 6.0 V	-	22	39	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	23	-	ns
	propagation delay An or Bn to Sn	see Figure 6				
		V_{CC} = 2.0 V	-	69	210	ns
		V_{CC} = 4.5 V	-	25	42	ns
		V_{CC} = 6.0 V	-	20	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	ns
	propagation delay CIN to COUT	see Figure 6				
		V_{CC} = 2.0 V	-	63	195	ns
		V_{CC} = 4.5 V	-	23	39	ns
		V_{CC} = 6.0 V	-	18	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	ns
	propagation delay An or Bn to COUT	see Figure 6				
		V_{CC} = 2.0 V	-	63	195	ns
		V_{CC} = 4.5 V	-	23	39	ns
		V_{CC} = 6.0 V	-	18	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{THL}, t_{TLH}	output transition time	see Figure 6					
		V_{CC} = 2.0 V		-	19	75	ns
		V_{CC} = 4.5 V		-	7	15	ns
		V_{CC} = 6.0 V		-	6	13	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[1]	-	88	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay CIN to S1	see Figure 6					
		V_{CC} = 2.0 V		-	-	200	ns
		V_{CC} = 4.5 V		-	-	40	ns
		V_{CC} = 6.0 V		-	-	34	ns
	propagation delay CIN to S2	see Figure 6					
		V_{CC} = 2.0 V		-	-	225	ns
		V_{CC} = 4.5 V		-	-	45	ns
		V_{CC} = 6.0 V		-	-	38	ns
	propagation delay CIN to S3	see Figure 6					
		V_{CC} = 2.0 V		-	-	245	ns
		V_{CC} = 4.5 V		-	-	49	ns
		V_{CC} = 6.0 V		-	-	42	ns
	propagation delay CIN to S4	see Figure 6					
		V_{CC} = 2.0 V		-	-	290	ns
		V_{CC} = 4.5 V		-	-	58	ns
		V_{CC} = 6.0 V		-	-	49	ns
	propagation delay An or Bn to Sn	see Figure 6					
		V_{CC} = 2.0 V		-	-	265	ns
		V_{CC} = 4.5 V		-	-	53	ns
		V_{CC} = 6.0 V		-	-	45	ns
	propagation delay CIN to COUT	see Figure 6					
		V_{CC} = 2.0 V		-	-	245	ns
		V_{CC} = 4.5 V		-	-	49	ns
		V_{CC} = 6.0 V		-	-	42	ns
	propagation delay An or Bn to COUT	see Figure 6					
		V_{CC} = 2.0 V		-	-	245	ns
		V_{CC} = 4.5 V		-	-	49	ns
		V_{CC} = 6.0 V		-	-	42	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6					
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	16	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CIN to S1	see Figure 6				
		V_{CC} = 2.0 V	-	-	240	ns
		V_{CC} = 4.5 V	-	-	48	ns
		V_{CC} = 6.0 V	-	-	41	ns
	propagation delay CIN to S2	see Figure 6				
		V_{CC} = 2.0 V	-	-	270	ns
		V_{CC} = 4.5 V	-	-	54	ns
		V_{CC} = 6.0 V	-	-	46	ns
	propagation delay CIN to S3	see Figure 6				
		V_{CC} = 2.0 V	-	-	295	ns
		V_{CC} = 4.5 V	-	-	59	ns
		V_{CC} = 6.0 V	-	-	50	ns
	propagation delay CIN to S4	see Figure 6				
		V_{CC} = 2.0 V	-	-	345	ns
		V_{CC} = 4.5 V	-	-	69	ns
		V_{CC} = 6.0 V	-	-	59	ns
	propagation delay An or Bn to Sn	see Figure 6				
		V_{CC} = 2.0 V	-	-	315	ns
		V_{CC} = 4.5 V	-	-	63	ns
		V_{CC} = 6.0 V	-	-	54	ns
	propagation delay CIN to COUT	see Figure 6				
		V_{CC} = 2.0 V	-	-	295	ns
		V_{CC} = 4.5 V	-	-	59	ns
		V_{CC} = 6.0 V	-	-	50	ns
	propagation delay An or Bn to COUT	see Figure 6				
		V_{CC} = 2.0 V	-	-	295	ns
		V_{CC} = 4.5 V	-	-	59	ns
		V_{CC} = 6.0 V	-	-	50	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

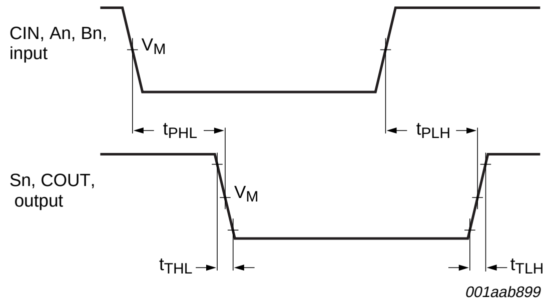
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

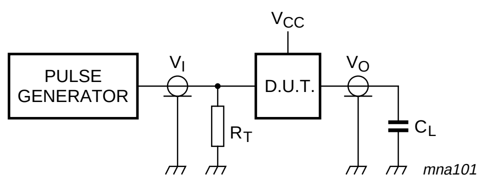
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

12. Waveforms



$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the inputs (CIN, An and Bn) to the outputs (Sn and COUT) propagation delays and the output transition times



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for switching times

Table 9: Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

13. Application information

Figure 8 shows a 3-bit adder using the 74HC283. Trying the operand inputs of the fourth adder (A4 and B4) LOW makes S4 dependent on, and equal to, the carry from the third adder.

Figure 9, based on the same principle, shows a method of dividing the 74HC283 into a 2-bit and 1-bit adder. The third stage adder (A3, B3 and S3) is used simply as means of transferring the carry into the fourth stage (via A3 and B3) and transferring the carry from the second stage on S3. As long as A3 and B3 are the same, HIGH or LOW, they do not influence S3. Similarly, when A3 and B3 are the same, the carry into the third stage does not influence the carry out of the third stage.

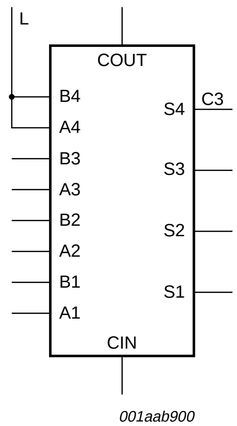


Fig 8. 3-bit adder

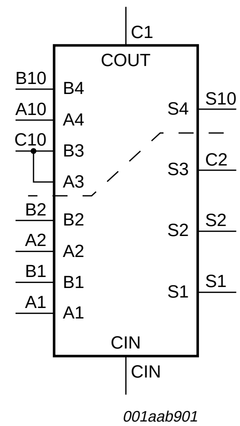


Fig 9. 2-bit and 1-bit adder

Figure 10 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S1, S2 and S3 produce a binary number equal to the number inputs (I1 to I5) that are HIGH.

Figure 11 shows a method of implementing a 5-input majority gate. When three or more inputs (I1 to I5) are HIGH, the output M5 is HIGH.

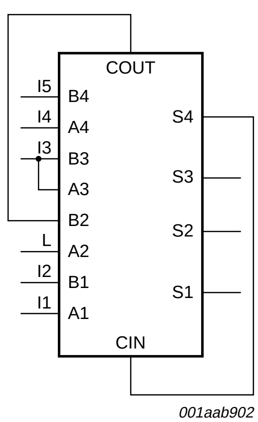


Fig 10. 5-input encoder

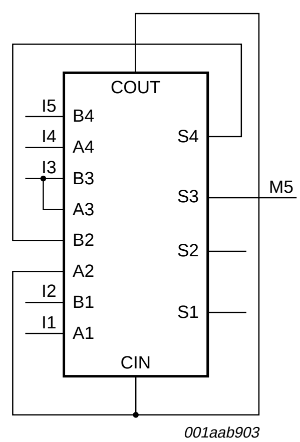
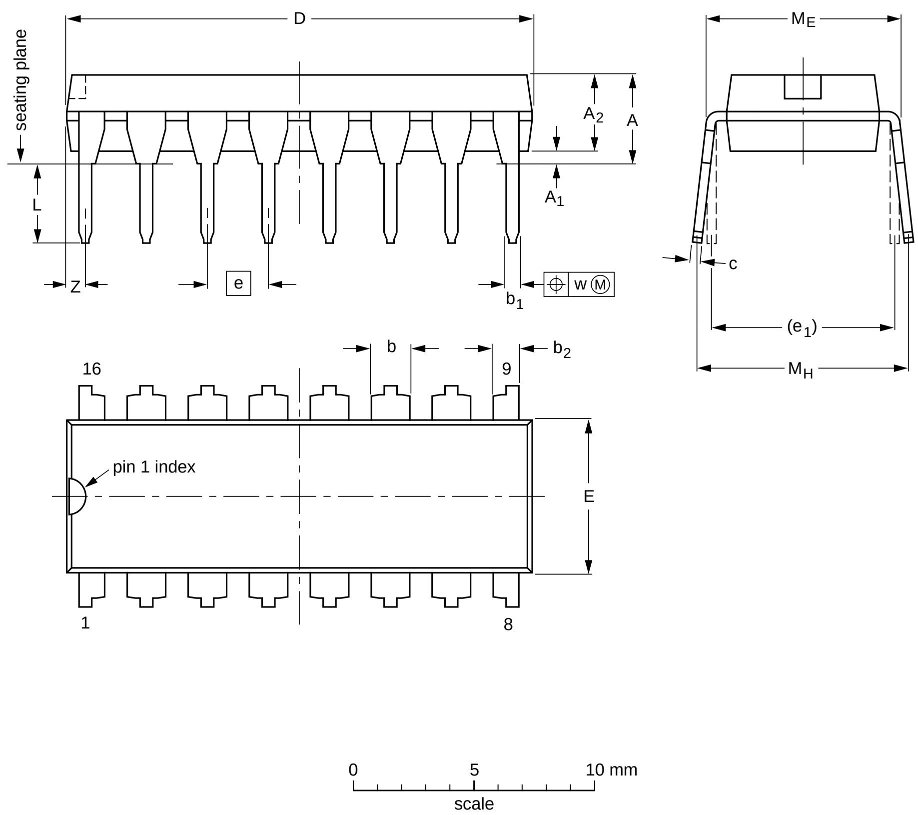


Fig 11. 5-input majority gate

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

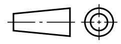
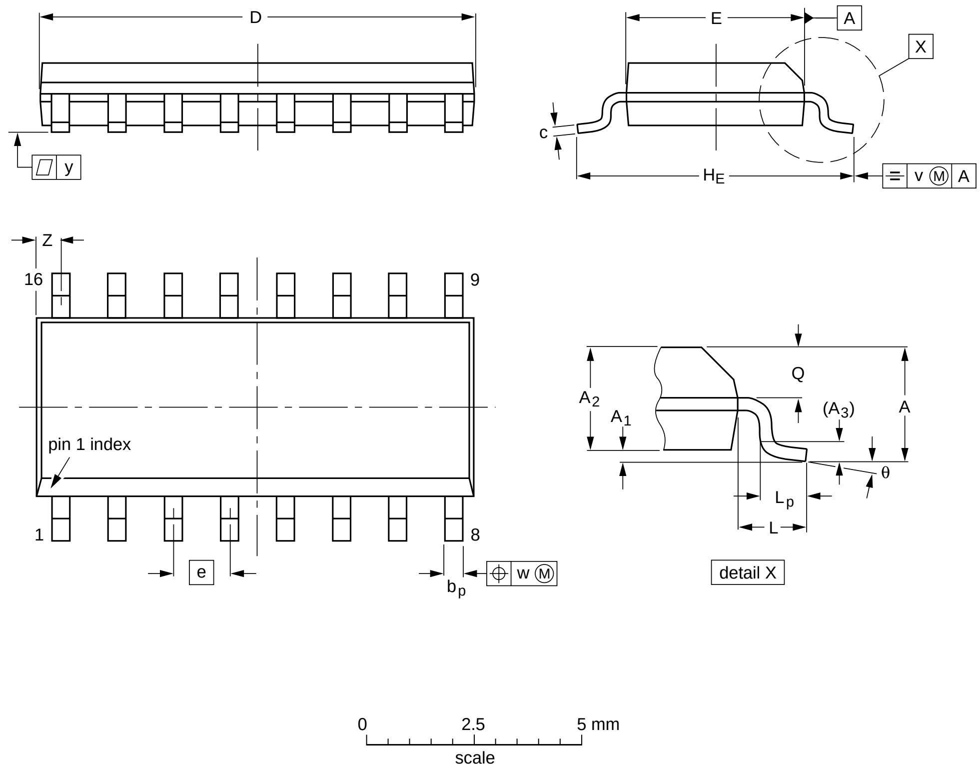
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 12. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

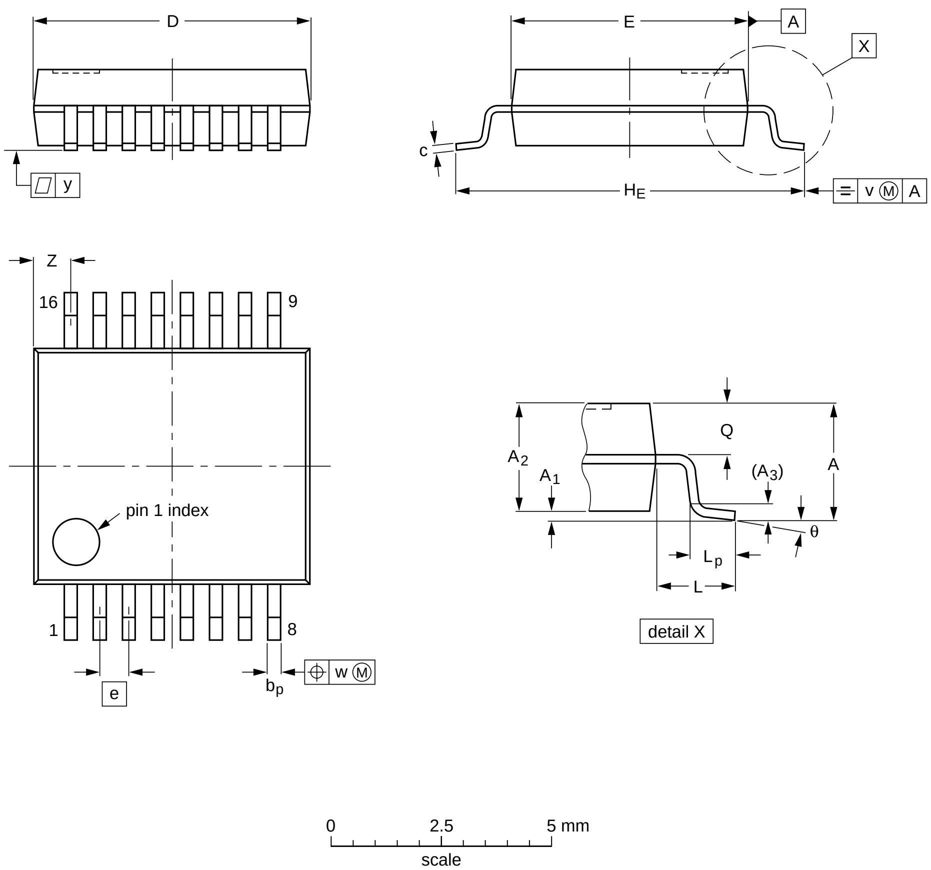
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(1)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

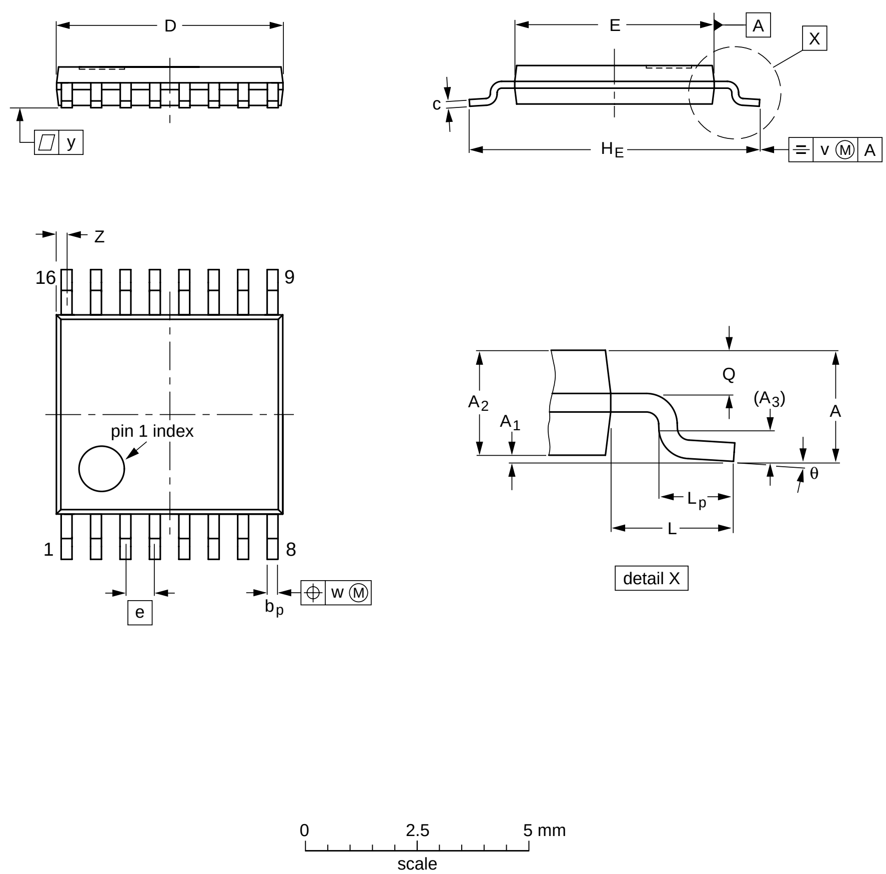
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

15. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC283_3	20041111	Product data sheet	-	9397 750 13811	74HC_HCT283_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT283. • Inserted family specification.				
74HC_HCT283_CNV_2	19970828	Product specification	-	-	74HC_HCT283_1
74HC_HCT283_1	19901201	Product specification	-	-	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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