

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT166

8-bit parallel-in/serial-out shift register

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit parallel-in/serial-out shift register

## 74HC/HCT166

## FEATURES

- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- Clock enable for “do nothing” mode
- Asynchronous master reset
- For asynchronous parallel data load see “165”
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by

an active LOW parallel enable ( $\overline{PE}$ ) input. When  $\overline{PE}$  is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When  $\overline{PE}$  is HIGH, data is entered into the internal bit position  $Q_0$  from serial data input ( $D_S$ ), and the remaining bits are shifted one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition.

This feature allows parallel-to-serial converter expansion by tying the  $Q_7$  output to the  $D_S$  input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input  $\overline{CE}$  should only take place while CP is HIGH for predictable operation. A LOW on the master reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>7</sub> MR to Q <sub>7</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	15 14	20 19	ns ns
f <sub>max</sub>	maximum clock frequency		63	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	41	41	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

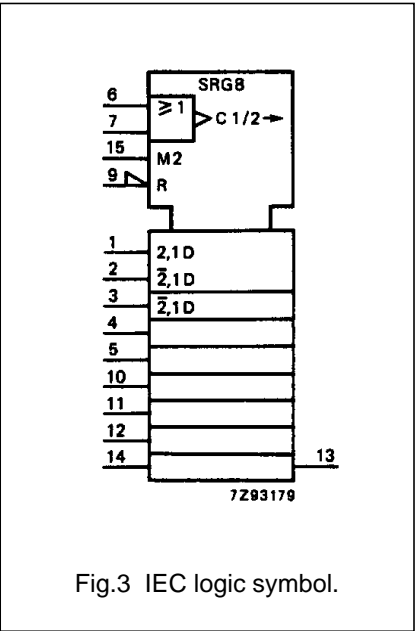
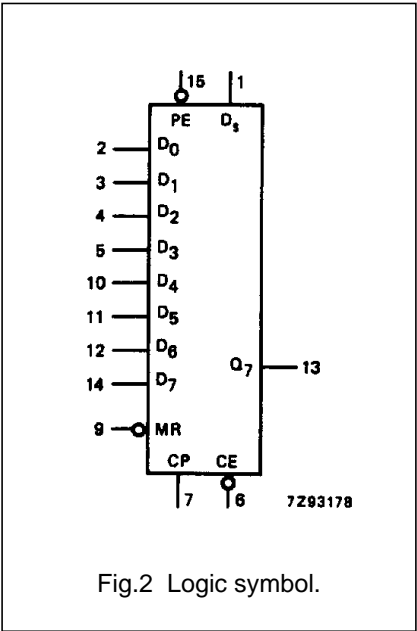
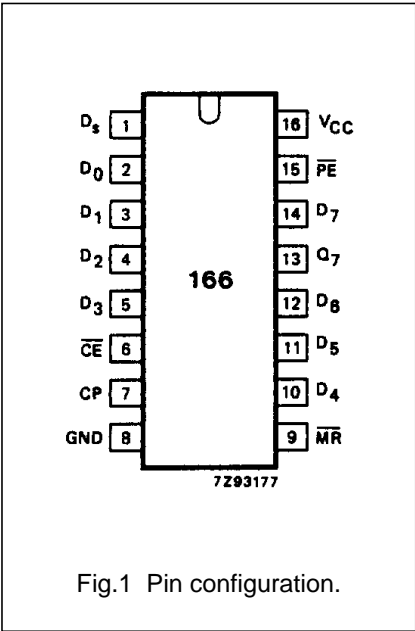
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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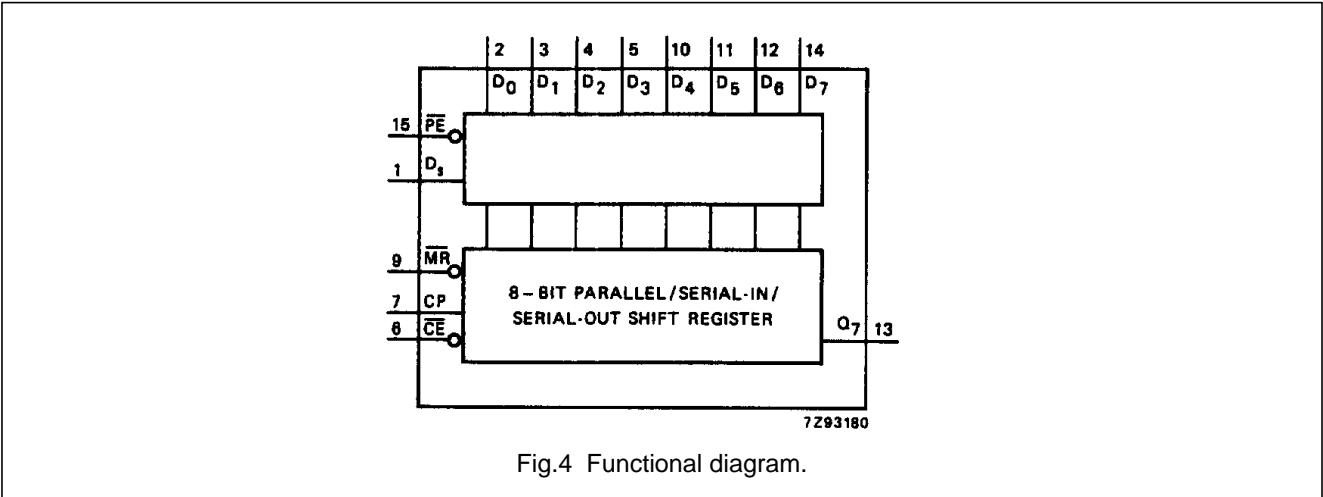
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	D <sub>s</sub>	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
6	$\overline{\text{CE}}$	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	$\overline{\text{MR}}$	asynchronous master reset (active LOW)
13	Q <sub>7</sub>	serial output from the last stage
15	$\overline{\text{PE}}$	parallel enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage



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FUNCTION TABLE

OPERATING MODES	INPUTS					Q <sub>n</sub> REGISTER		OUTPUT
	$\overline{\text{PE}}$	$\overline{\text{CE}}$	CP	D <sub>S</sub>	D <sub>0</sub> -D <sub>7</sub>	Q <sub>0</sub>	Q <sub>1</sub> -Q <sub>6</sub>	Q <sub>7</sub>
parallel load	L	L	↑	X	L - L	L	L - L	L
	L	L	↑	X	h - h	H	H - H	H
serial shift	h	L	↑	L	X - X	L	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>
	h	L	↑	h	X - X	H	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>
hold "do nothing"	X	h	X	X	X - X	q <sub>0</sub>	q <sub>1</sub> - q <sub>6</sub>	q <sub>7</sub>

Notes

1.
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- L = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

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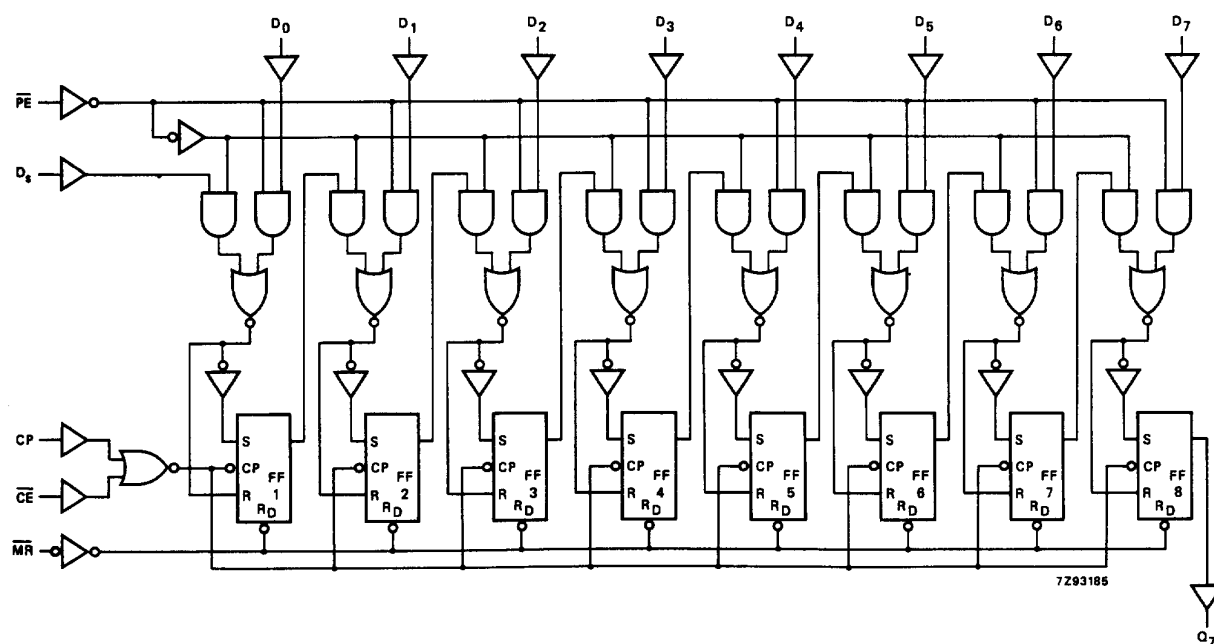


Fig.5 Logic diagram.

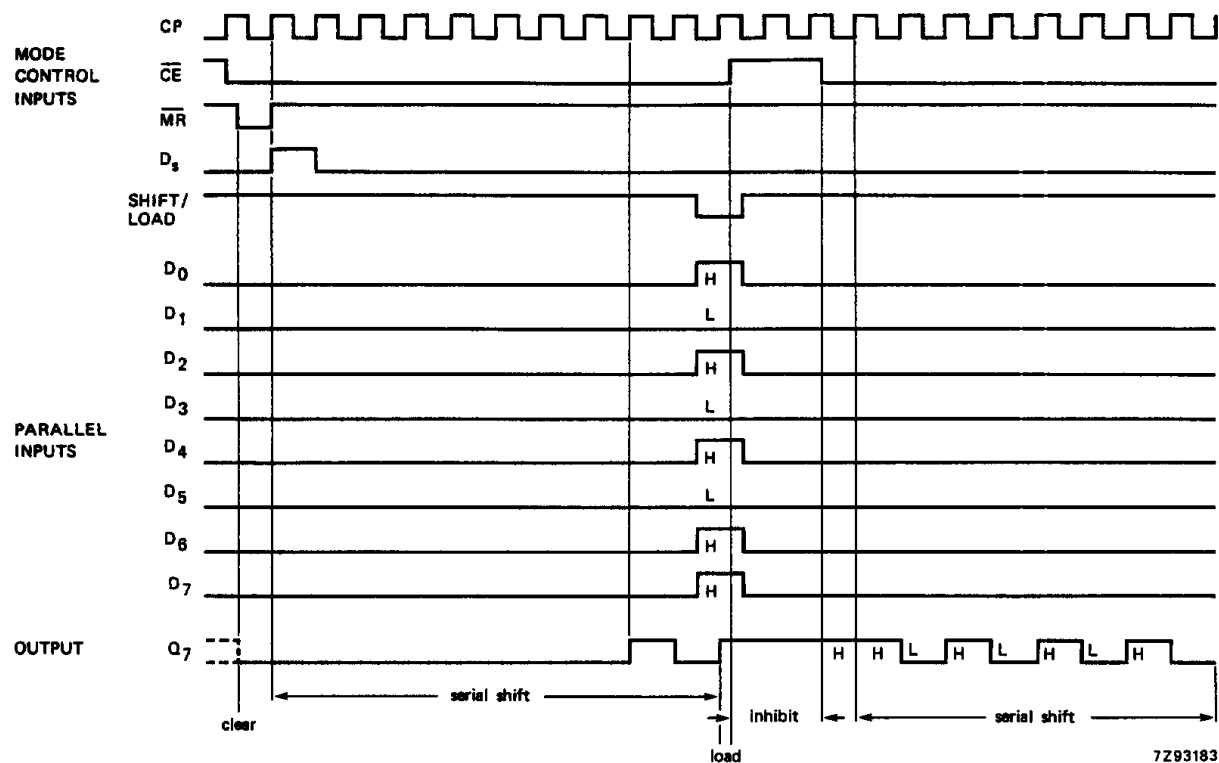


Fig.6 Typical clear, shift, load, inhibit, and shift sequences.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>7</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub>	propagation delay MR to Q <sub>7</sub>		47 17 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>W</sub>	master reset pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t <sub>rem</sub>	removal time MR to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> , CE to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t <sub>su</sub>	set-up time PE to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> , CE to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time PE to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.9
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>0</sub> to D <sub>7</sub>	0.35
D <sub>s</sub>	0.35
CP	0.80
$\overline{CE}$	0.80
$\overline{MR}$	0.40
$\overline{PE}$	0.60

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## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>7</sub>		23	40		50		60	ns	4.5	Fig.7
t <sub>PHL</sub>	propagation delay $\overline{MR}$ to Q <sub>7</sub>		22	40		50		60	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.7
t <sub>W</sub>	clock pulse width HIGH or LOW	20	9		25		30		ns	4.5	Fig.7
t <sub>W</sub>	master reset pulse width LOW	25	11		31		38		ns	4.5	Fig.8
t <sub>rem</sub>	removal time $\overline{MR}$ to CP	0	−7		0		0		ns	4.5	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> , $\overline{CE}$ to CP	16	8		20		24		ns	4.5	Fig.9
t <sub>su</sub>	set-up time $\overline{PE}$ to CP	30	15		38		45		ns	4.5	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> , $\overline{CE}$ to CP	0	−3		0		0		ns	4.5	Fig.9
t <sub>h</sub>	hold time $\overline{PE}$ to CP	0	−13		0		0		ns	4.5	Fig.9
f <sub>max</sub>	maximum clock pulse width	25	45		20		17		MHz	4.5	Fig.7



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## AC WAVEFORMS

The changing to output assumes internal  $Q_6$  opposite state from  $Q_7$ .

The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the function table.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND to } 3V$ .

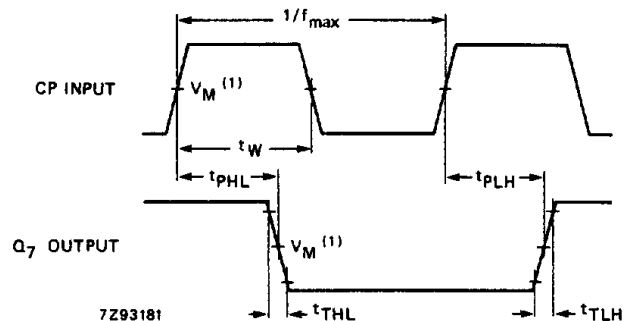


Fig.7 Waveforms showing the clock (CP) to output ( $Q_7$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the function table.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND to } 3V$ .

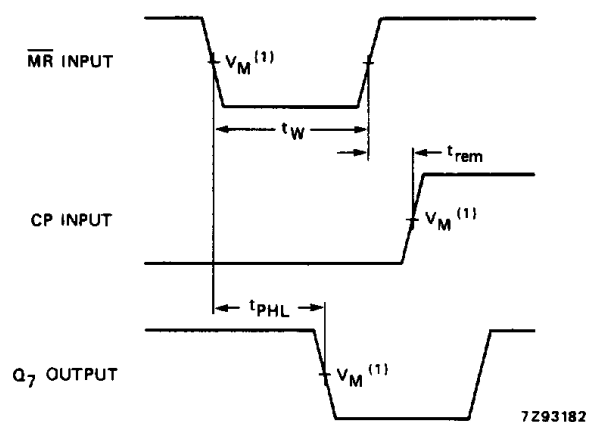
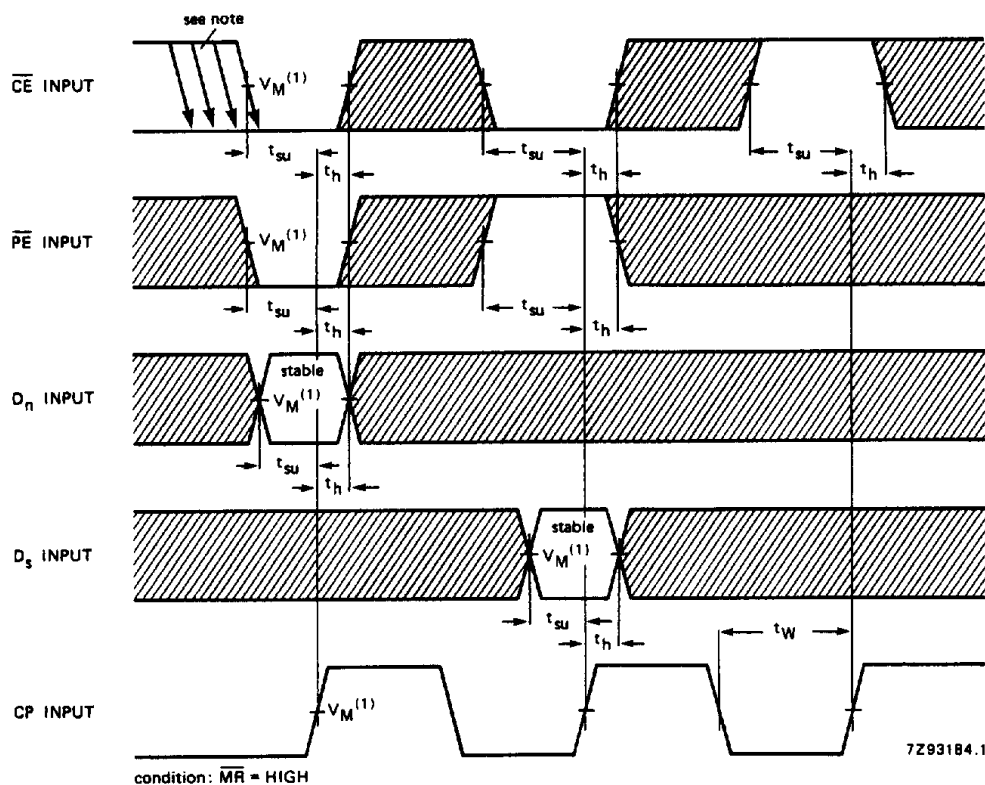


Fig.8 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_7$ ) propagation delay and the master reset to clock (CP) removal time.

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The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the function table.

$\overline{CE}$  may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND to } 3V$ .

Fig.9 Waveforms showing the set-up and hold times from the serial data input ( $D_s$ ), the data inputs ( $D_n$ ), the clock enable input (LOW  $\overline{CE}$ ), the clock enable input  $\overline{CE}$  and the parallel enable input to the clock (CP).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".