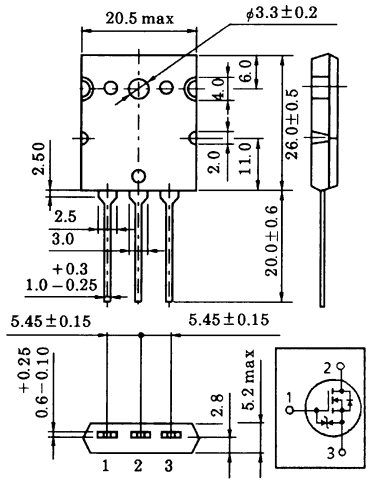
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSV)

2SK3131

Chopper Regulator DC−DC Converter and Motor Drive Applications

- Fast reverse recovery time : t_{rr} = 105 ns (typ.)
- Built-in high-speed free-wheeling diode
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.085 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 35 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 500 V)
- Enhancement mode : V_{th} = 2.4~3.4 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



1.GATE
2.DRAIN (heat sink)
3.SOURCE

JEDEC	—
JEITA	—
TOSHIBA	2-21F1B

Weight: 9.75 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	500	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	500	V
Gate−source voltage		V_{GSS}	±30	V
DC Drain current	DC (Note 1)	I_D	50	A
	Pulse (Note 1)	I_{DP}	200	A
Drain power dissipation (Tc = 25°C)		P_D	250	W
Single pulse avalanche energy (Note 2)		E_{AS}	525	mJ
Avalanche current		I_{AR}	50	A
Repetitive avalanche energy (Note 3)		E_{AR}	25	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	0.5	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	35.7	°C / W

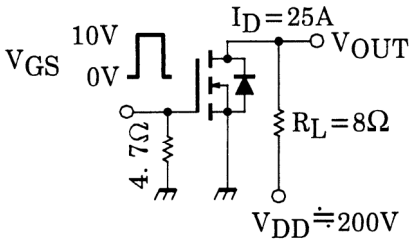
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 357 μH, R_G = 25 Ω, I_{AR} = 50 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device.
Please handle with caution.

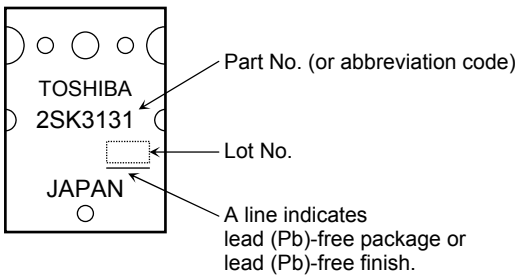
Electrical Characteristics (Ta = 25°C)

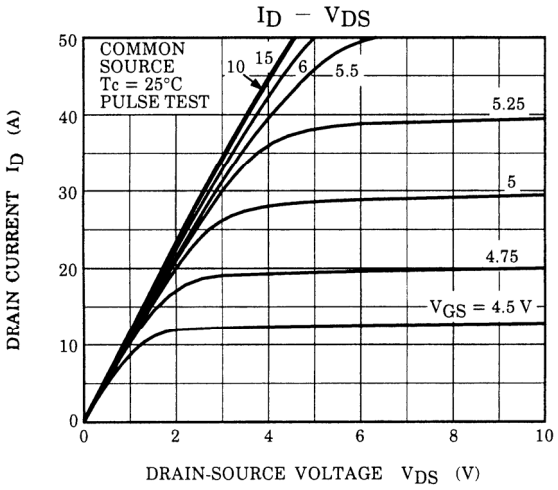
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate−source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±100 μA, V_{DS} = 0 V	±30	—	—	V
Drain cut−off current		I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	500	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.4	—	3.4	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 25 A	—	0.085	0.11	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 25 A	15	35	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	11000	—	pF
Reverse transfer capacitance		C_{rss}		—	2100	—	
Output capacitance		C_{oss}		—	4200	—	
Switching time	Rise time	tr		—	105	—	ns
	Turn−on time	t_{on}		—	160	—	
	Fall time	t_f		—	65	—	
	Turn−off time	t_{off}		—	245	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 50 A	—	280	—	nC
Gate−source charge		Q_{gs}		—	150	—	
Gate−drain (“miller”) charge		Q_{gd}		—	130	—	

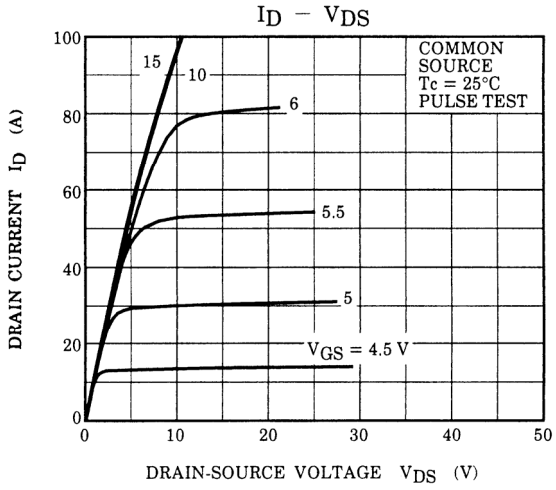
Source−Drain Ratings and Characteristics (Ta = 25°C)

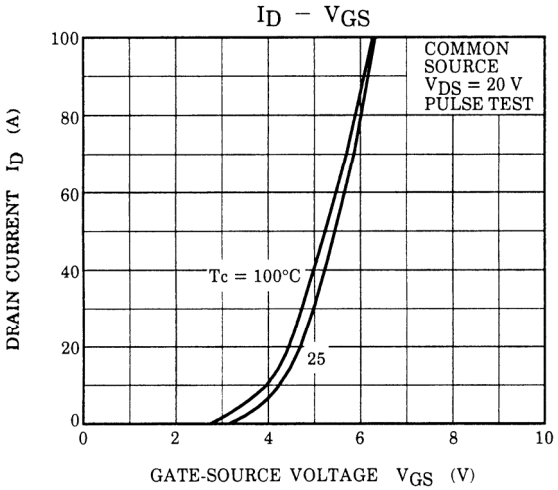
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	50	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	200	A
Forward voltage (diode)	V_{DSF}	V_{DR} = 25 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 50 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	105	—	ns
Reverse recovery charge	Q_{rr}		—	380	—	nC

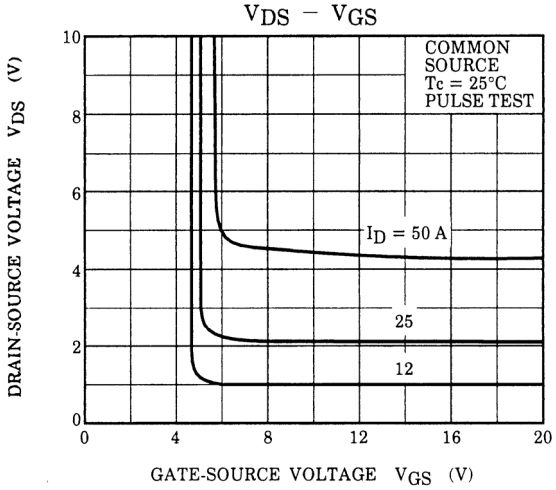
Marking

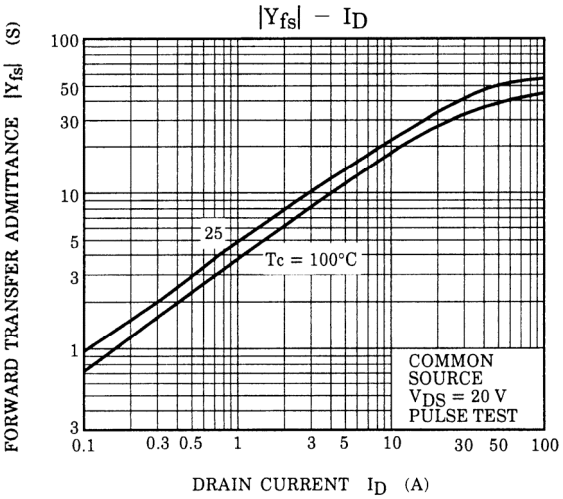


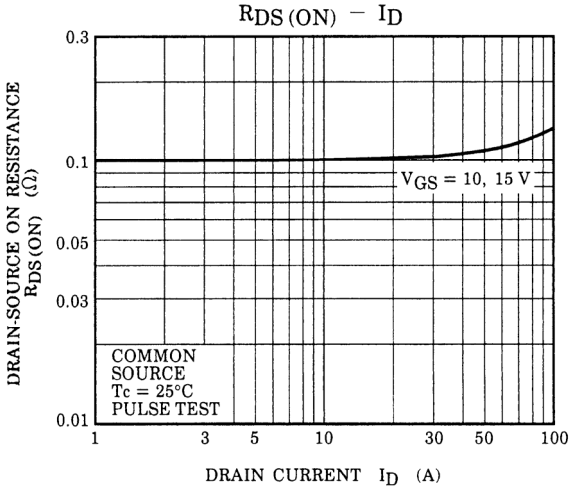

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
10
6
5.5
5.25
5
4.75
V_{GS} = 4.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
10
6
5.5
5
V_{GS} = 4.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)

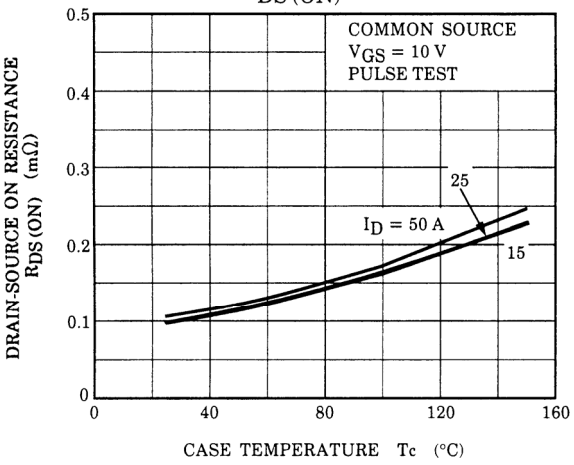

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
Tc = 100°C
25
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)


V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 50 A
25
12
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)

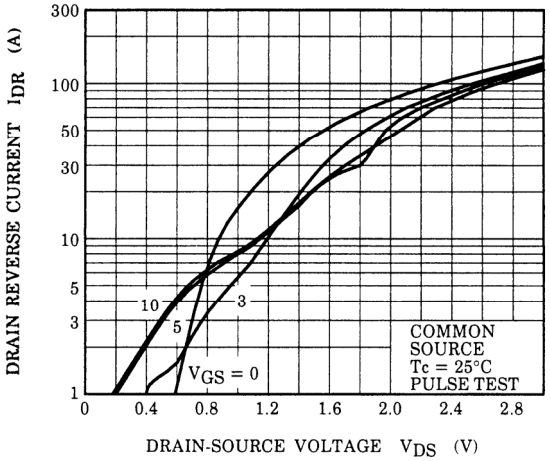

$|Y_{fs}|$ – I_D
25
Tc = 100°C
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS\,(ON)}$ – I_D
V_{GS} = 10, 15 V
COMMON SOURCE
Tc = 25°C
PULSE TEST
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT I_D (A)

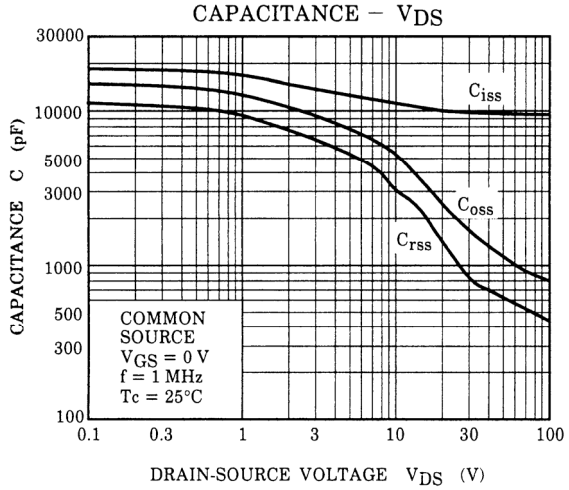
$R_{DS\,(ON)}$ – Tc



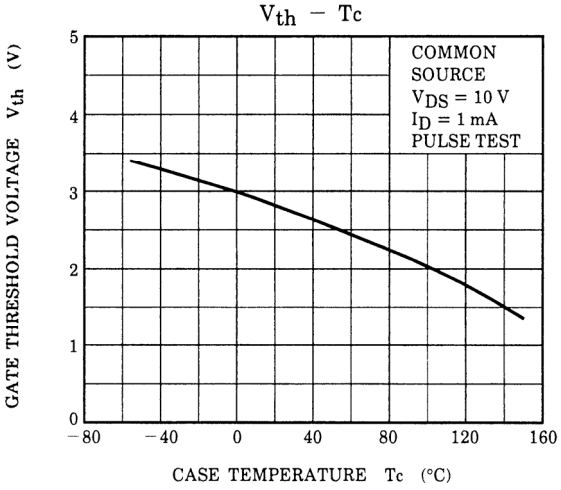
I_{DR} – V_{DS}



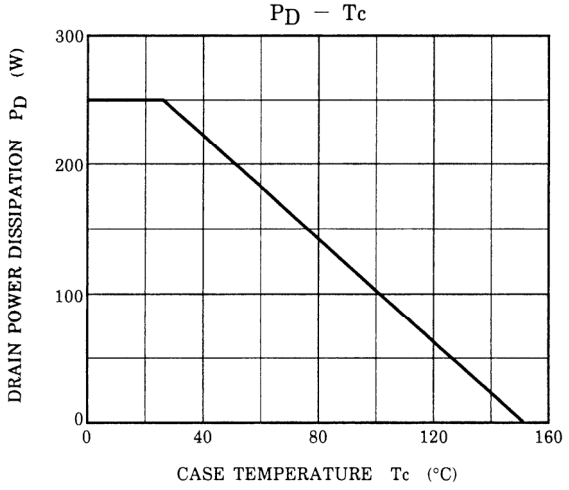
CAPACITANCE – V_{DS}



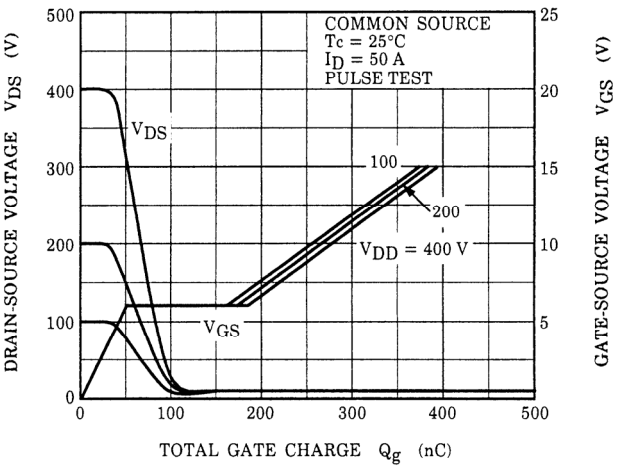
V_{th} – Tc



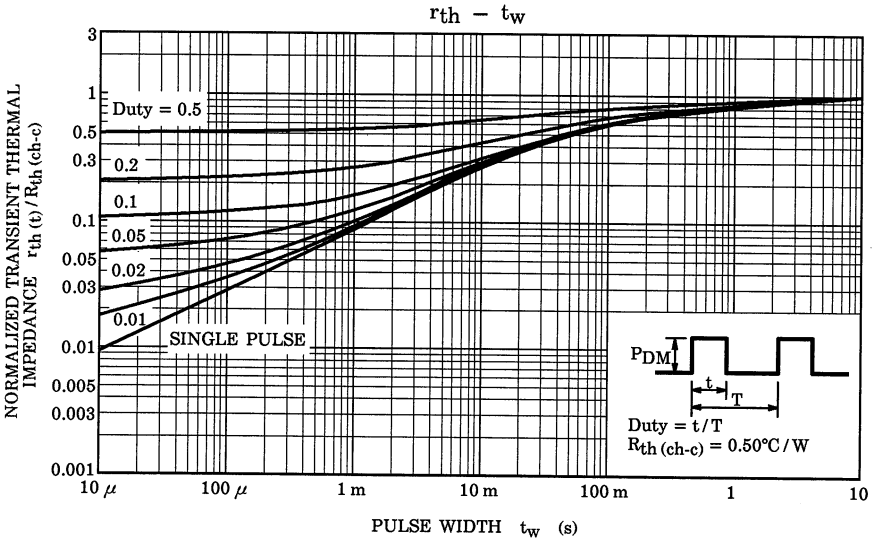
P_D – Tc



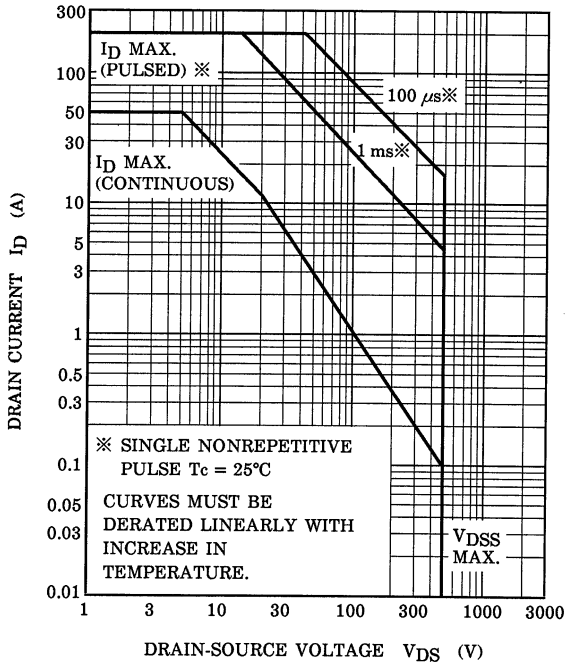
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



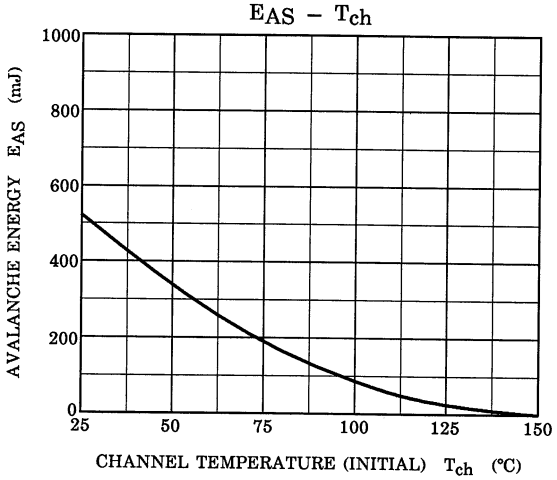
$r_{th} - t_w$

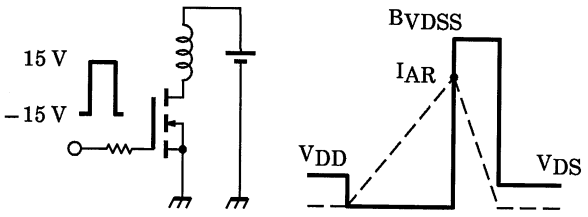


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 357 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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