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MOS FIELD EFFECT POWER TRANSISTOR

2SK1294

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1294 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 27 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$)
 $R_{DS(on)} \leq 50 \text{ m}\Omega$ ($V_{GS} = 4 \text{ V}$, $I_D = 20 \text{ A}$)
- Low C_{iss} $C_{iss} = 3 \text{ 250 pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

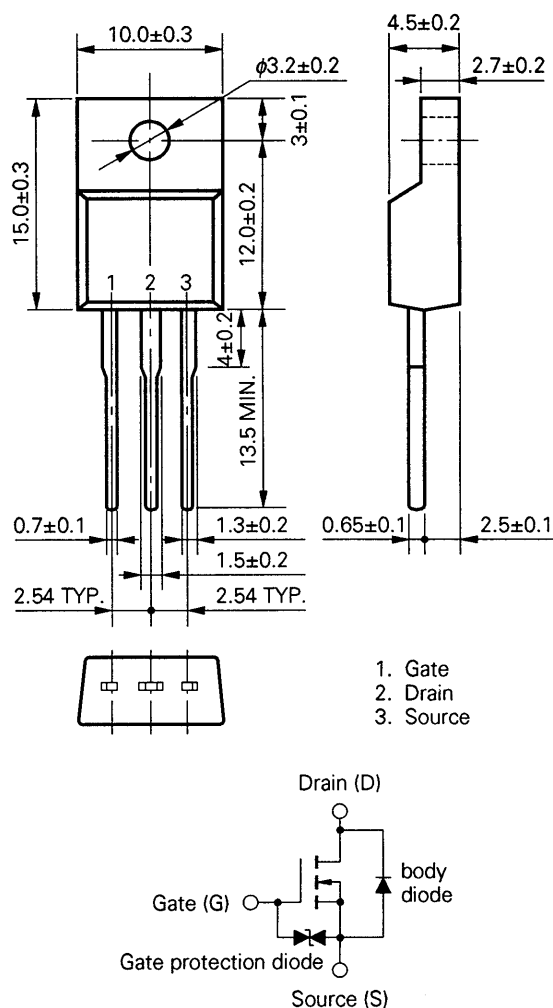
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 40	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 160	A
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T1}	2.0	W
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T2}	35	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS

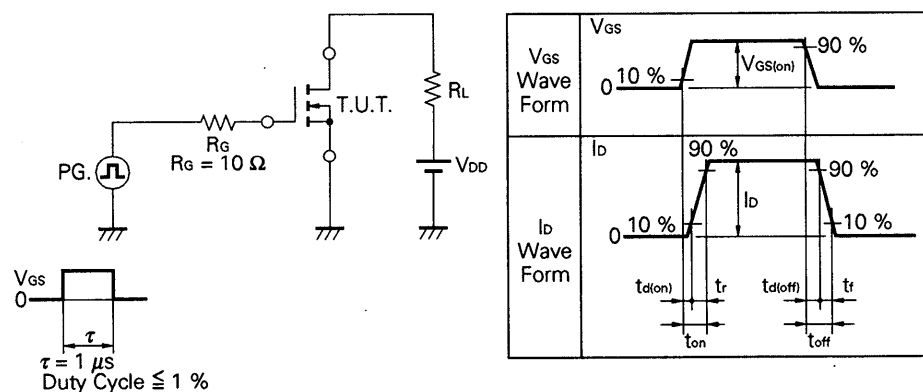
(in millimeters)



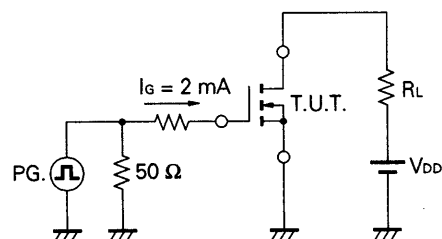
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		22	27	$\text{m}\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		30	50	$\text{m}\Omega$	$V_{GS} = 4.0\text{ V}$, $I_D = 15\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	12			S	$V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$
Drain Leakage Current	I_{DSS}			10	μA	$V_{DS} = 60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		3 250		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		1 200		pF	
Reverse Transfer Capacitance	C_{res}		380		pF	
Turn-On Delay Time	$t_{d(on)}$		60		ns	$V_{GS(on)} = 10\text{ V}$ $V_{DD} = 30\text{ V}$ $I_D = 20\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 1.5\text{ }\Omega$
Rise Time	t_r		500		ns	
Turn-Off Delay Time	$t_{d(off)}$		250		ns	
Fall Time	t_f		160		ns	
Total Gate Charge	Q_G		85		nC	$V_{GS} = 10\text{ V}$ $I_D = 40\text{ A}$ $V_{DD} = 48\text{ V}$
Gate to Source Charge	Q_{GS}		10		nC	
Gate to Drain Charge	Q_{GD}		35		nC	
Diode Forward Voltage	V_{SD}		1.2		V	$I_{SD} = 40\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		130		ns	$I_F = 40\text{ A}$, $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		200		nC	

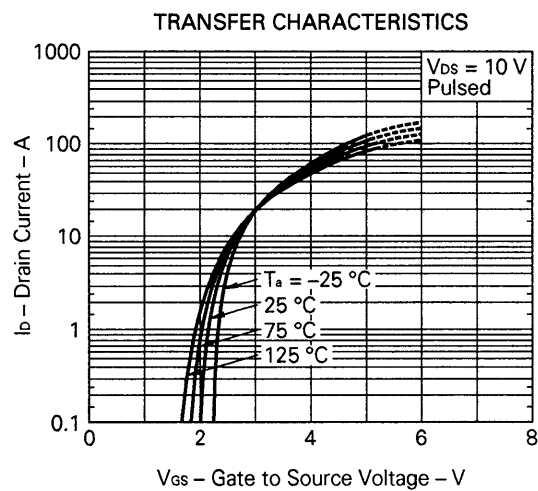
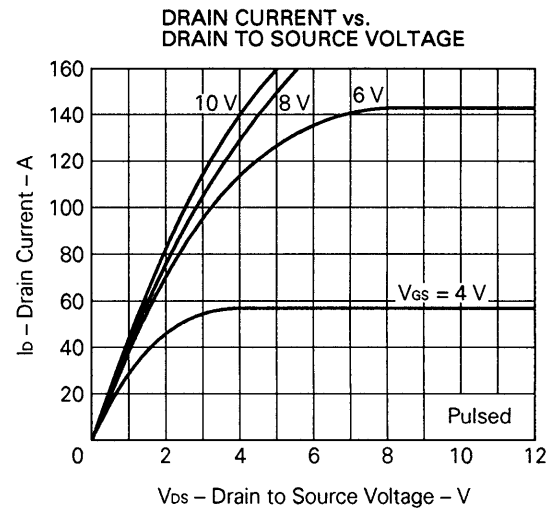
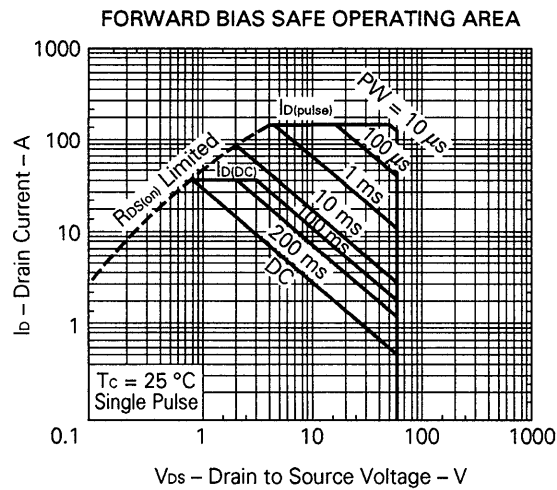
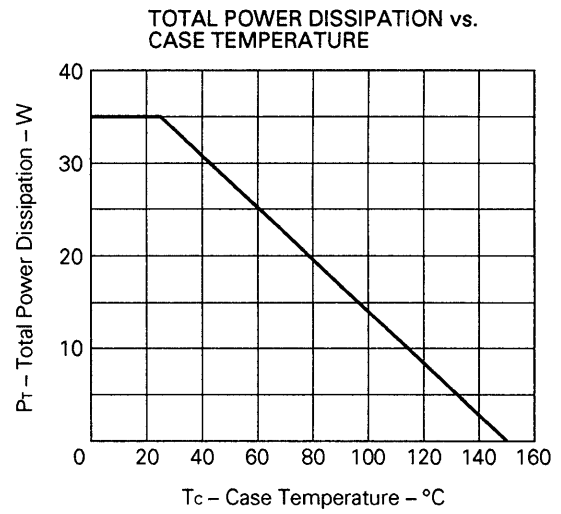
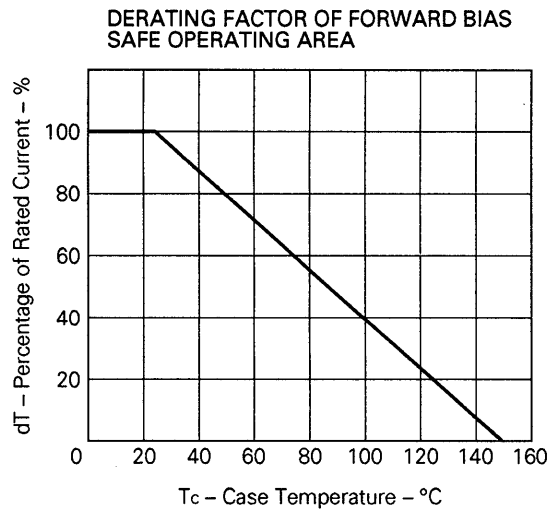
Test Circuit 1: Switching Time



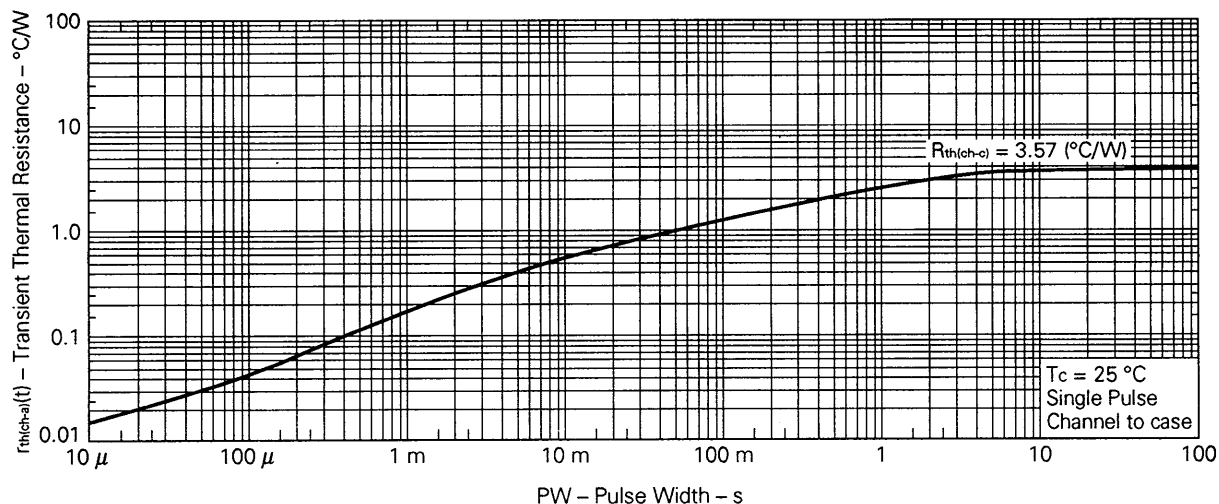
Test Circuit 2: Gate Charge



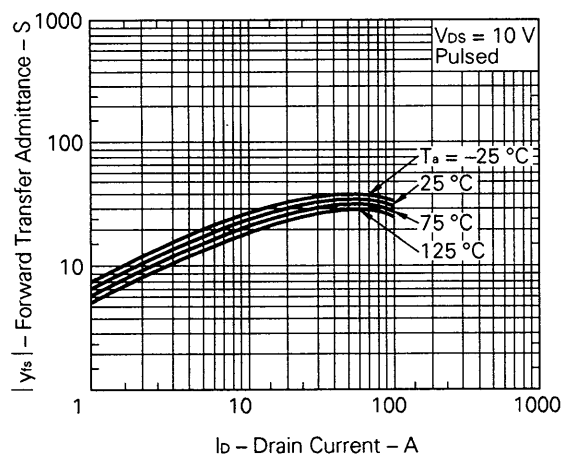
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



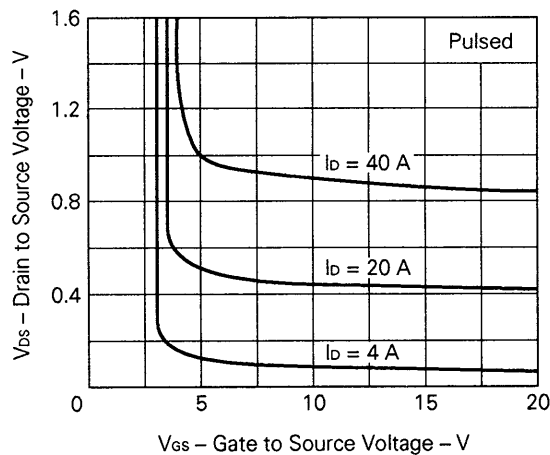
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



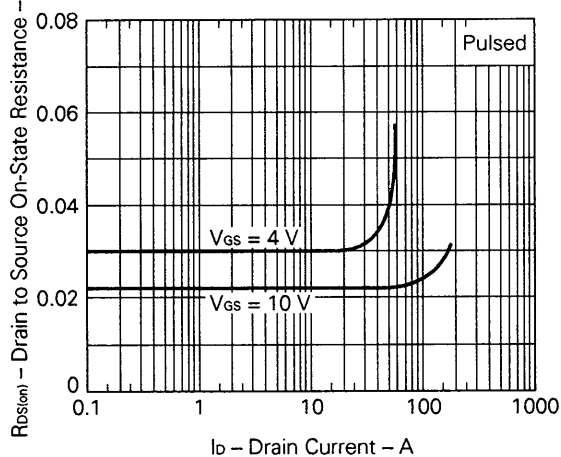
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



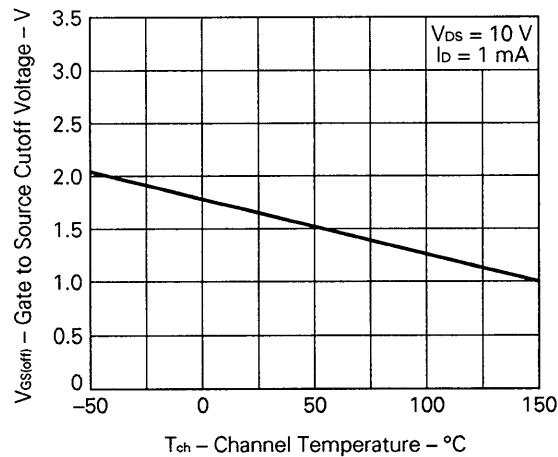
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

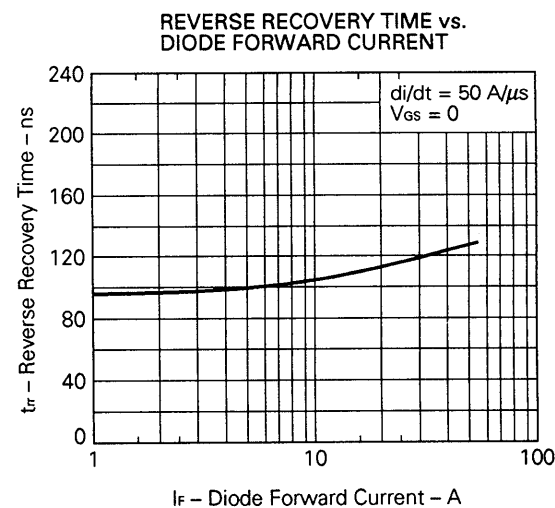
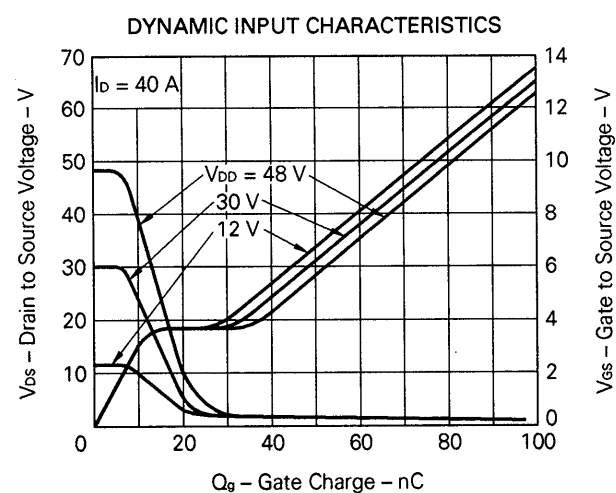
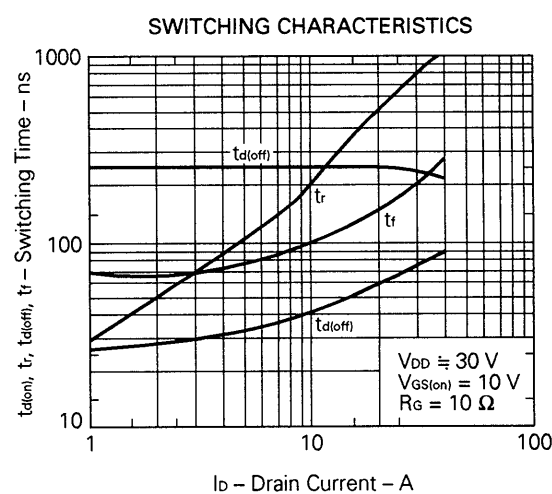
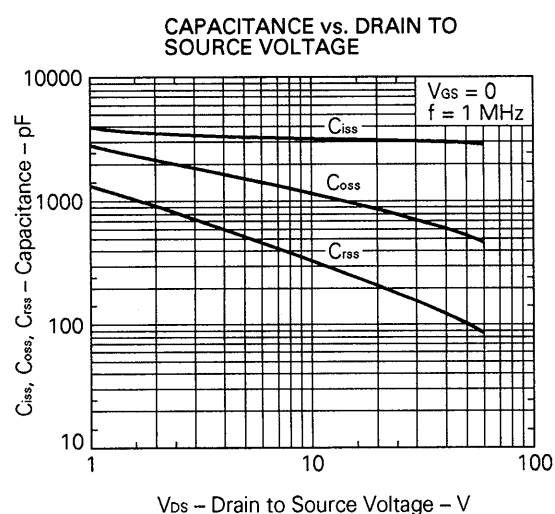
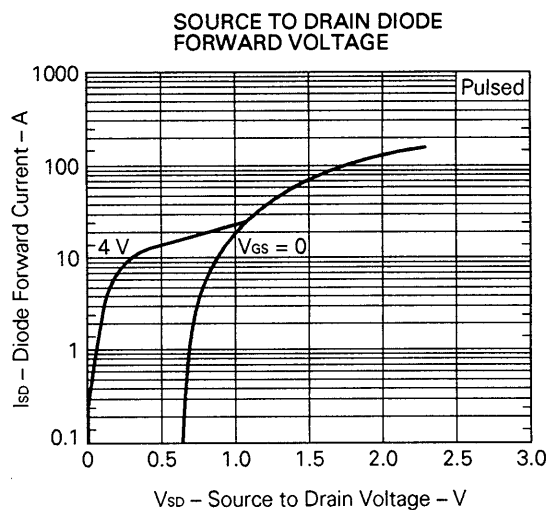
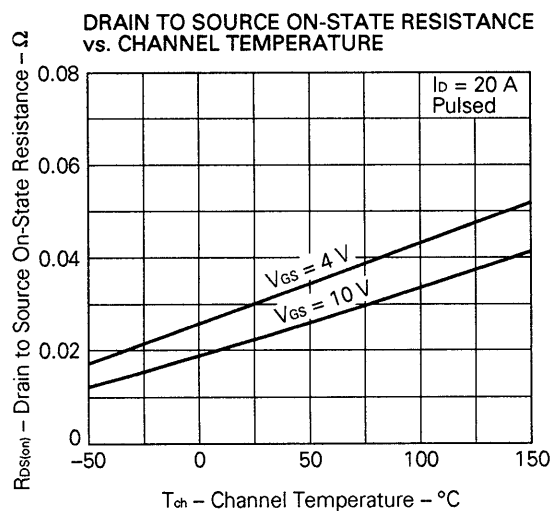


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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