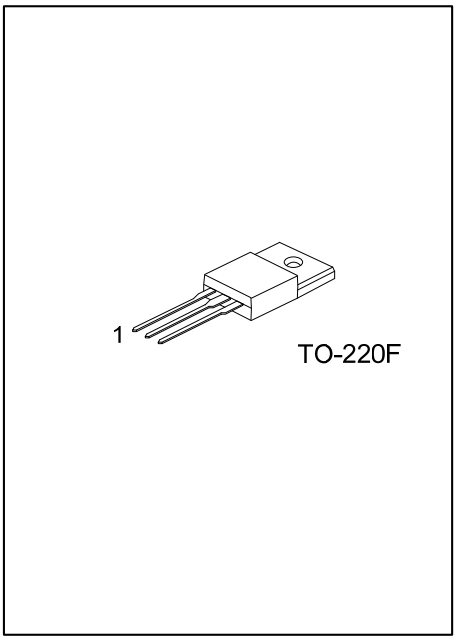
11N40

Power MOSFET

400 V N-CHANNEL MOSFET



Lead-free: 11N40L
Halogen-free: 11N40G

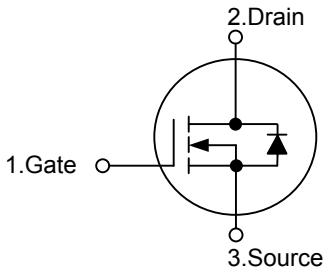
■ DESCRIPTION

The **11N40** uses UTC's advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

■ FEATURES

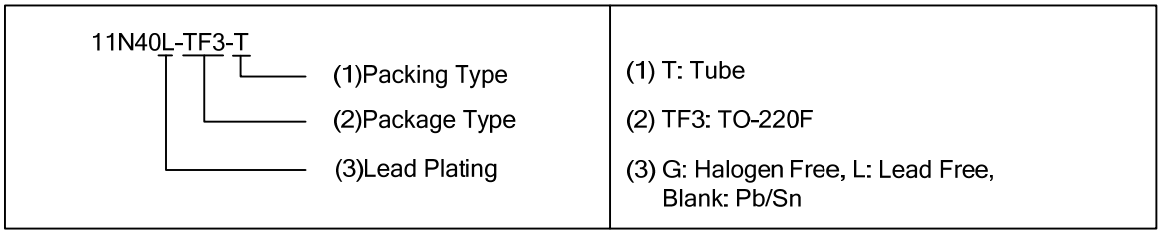
* $R_{DS(ON)}$ = 0.48Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 27 nC)
* Low reverse transfer capacitance (C_{RSS} = typical 20 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free Plating	Halogen Free		1	2	3	
11N40-TF3-T	11N40L-TF3-T	11N40G-TF3-T	TO-220F	G	D	S	Tube



■ ABSOLUTE MAXIMUM RATING (T_C =25℃, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	±30	V
Continuous Drain Current (T_C = 25℃)		I_D	11.4	A
Pulsed Drain Current (Note 1)		I_{DM}	46	A
Avalanche Current (Note 1)		I_{AR}	11.4	A
Avalanche Energy	Single Pulsed(Note 2)	E_{AS}	520	mJ
	Repetitive(Note 1)	E_{AR}	14.7	
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation		P_D	147	W
Derate above 25℃			1.18	W/℃
Junction Temperature		T_J	150	℃
Storage Temperature		T_{STG}	-55 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to- Ambient	θ_{JA}			62.5	℃/W
Junction-to-Case	θ_{JC}			0.85	℃/W

■ ELECTRICAL CHARACTERISTICS (T_J =25℃, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0 V, I_D =250 μA	400			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =400V, V_{GS} =0 V			1	μA
		V_{DS} =320V, T_C =125°C			10	
Gate-Body Leakage Current	I_{GSS}	V_{DS} =0 V, V_{GS} = ±30 V			±100	nA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D =250 μA, Referenced to25°C		0.42		mV/℃
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} =V_{GS}, I_D =250 μA	2.0		4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 5.7 A		0.38	0.48	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{DS} =25V, V_{GS} =0V, f=1MHz		1100	1400	pF
Output Capacitance	C_{OSS}			180	240	
Reverse Transfer Capacitance	C_{RSS}			20	30	
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	V_{DD}=200V, I_D=11.4A, R_{GEN} =25Ω(Note 4,5)		30	70	ns
Turn-ON Rise Time	t_R			100	210	
Turn-OFF Delay Time	$t_{D(OFF)}$			60	130	
Turn-OFF Fall-Time	t_F			60	130	
Total Gate Charge	Q_G	V_{DS} =320V, V_{GS} =10V, I_D =11.4A (Note 4,5)		27	35	nC
Gate Source Charge	Q_{GS}			7.3		
Gate Drain Charge	Q_{GD}			12.3		

■ ELECTRICAL CHARACTERISTICS(Cont.)

SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	I_S=11.4 A,V_{GS}=0V			1.5	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				11.4	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				46	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_F /dt = 100 A/ s,		240		ns
Reverse Recovery Charge	Q_{RR}	I_S = 11.4 A (Note 4)		1.8		µC

Note 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L=7mH, I_{AS}=11.4A, V_{DD}=50V, R_G=25Ω, Satarting T_J=25°C.
3. I_{SD} ≤ 11.4A, di/dt ≤ 200A/µs, V_{DD} ≤BV_{DSS}, Satarting T_J=25°C.
4. Pulse Test: Pulse Width ≤ 300 s, Duty Cycle ≤ 2%.
5. Independent of operating temperature.

■ TEST CIRCUIT

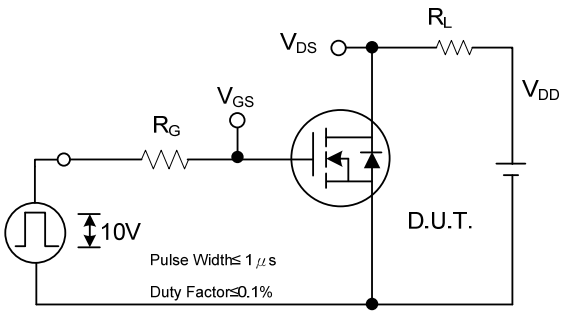


Fig. 2A Switching Test Circuit

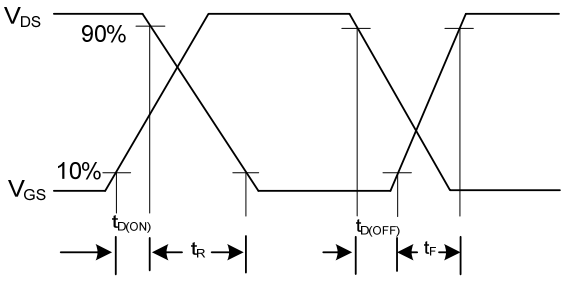


Fig. 2B Switching Waveforms

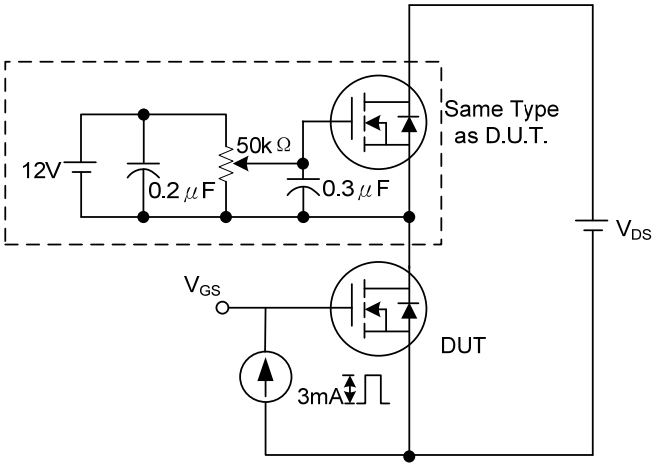


Fig. 3A Gate Charge Test Circuit

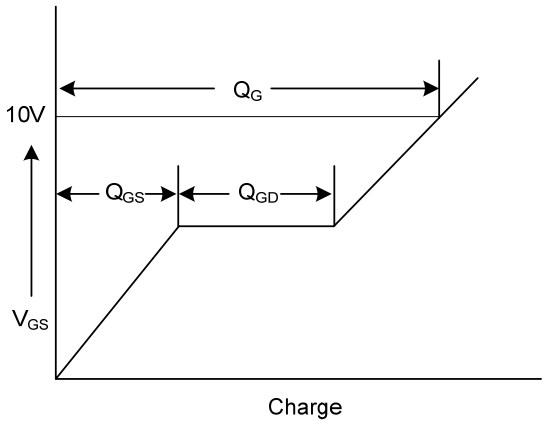


Fig. 3B Gate Charge Waveform

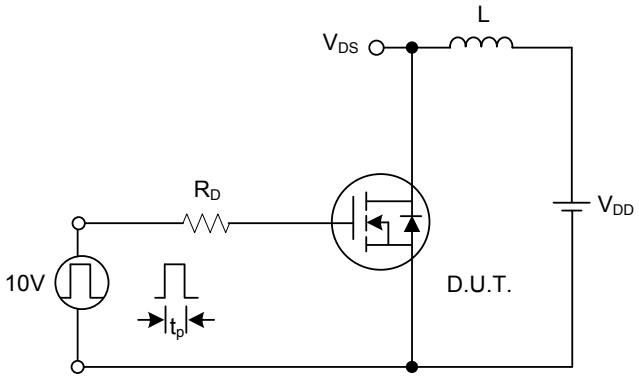


Fig. 4A Unclamped Inductive Switching Test Circuit

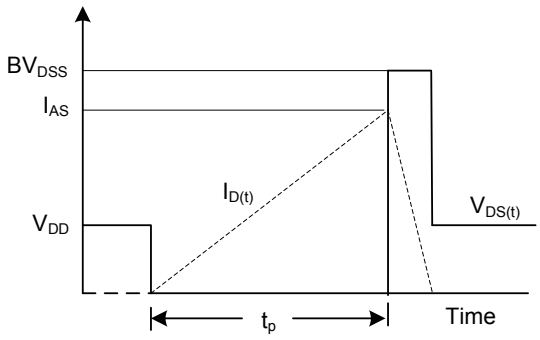


Fig. 4B Unclamped Inductive Switching Waveforms

■ TEST CIRCUIT(Cont.)

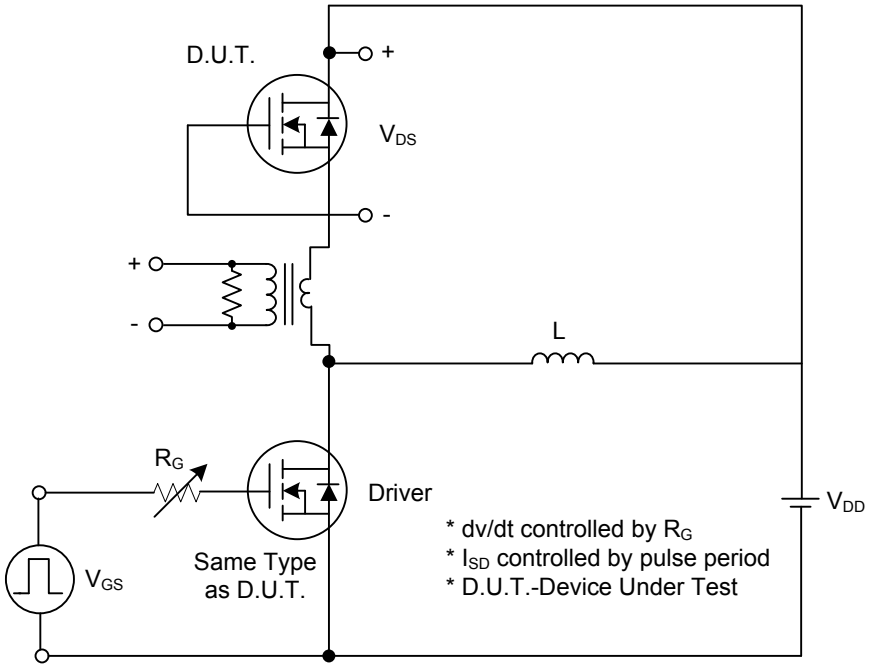


Fig. 1A Peak Diode Recovery dv/dt Test Circuit