



SPP4925B

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP4925B is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

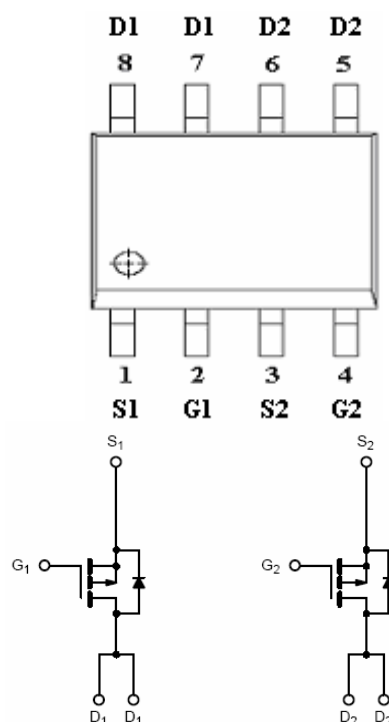
FEATURES

- ◆ -30V/-7.2A, $R_{DS(ON)} = 24m\Omega @ V_{GS} = -10V$
- ◆ -30V/-5.6A, $R_{DS(ON)} = 30m\Omega @ V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP4925BS8RGB	SOP- 8P	SPP4925B

※ SPP4925BS8RGB : 13" Tape Reel ; Halogen – Free ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	-7.2	A
		-5.6	
Pulsed Drain Current	I _{DM}	-20	A
Continuous Source Current(Diode Conduction)	I _S	-2.3	A
Power Dissipation	P _D	2.8	W
		1.8	
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	70	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.7		-1.6	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	uA
		V _{DS} =-24V, V _{GS} =0V T _J =85°C			-5	
On-State Drain Current	I _{D(on)}	V _{DS} = -5V, V _{GS} =-4.5V	-40			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-9.2A		0.020	0.024	Ω
		V _{GS} =-4.5V, I _D =-7.0A		0.024	0.030	
Forward Transconductance	g _{fs}	V _{DS} =-10V, I _D =-9.0A		24		S
Diode Forward Voltage	V _{SD}	I _S =-2.3A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-15V, V _{GS} =-10V I _D = -9.0A		20	30	nC
Gate-Source Charge	Q _{gs}			3.5		
Gate-Drain Charge	Q _{gd}			4.8		
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V f=1MHz		1850		pF
Output Capacitance	C _{oss}			450		
Reverse Transfer Capacitance	C _{rss}			335		
Turn-On Time	t _{d(on)}	V _{DD} =-15V, R _L =15Ω I _D =-1.0A, V _{GEN} =-10V R _G =6Ω		20	30	nS
	t _r			20	30	
Turn-Off Time	t _{d(off)}			75	110	
	t _f			40	80	

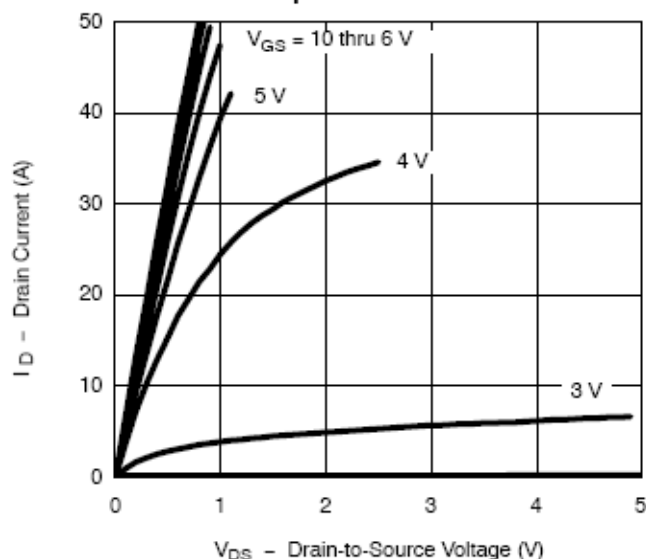


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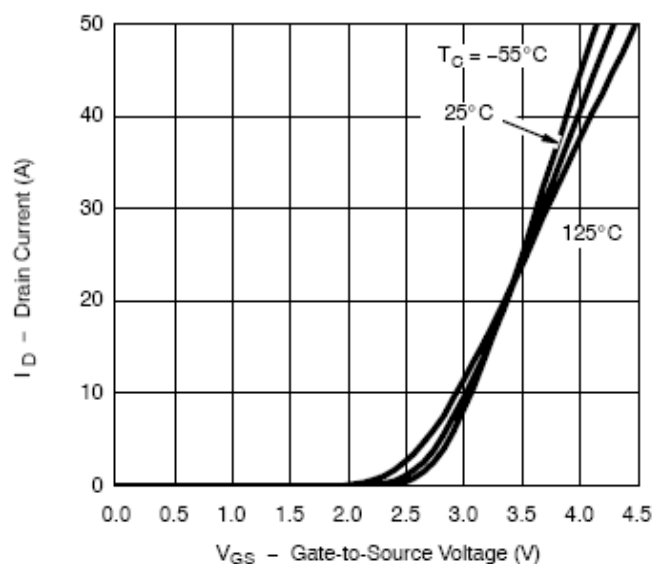
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TYPICAL CHARACTERISTICS

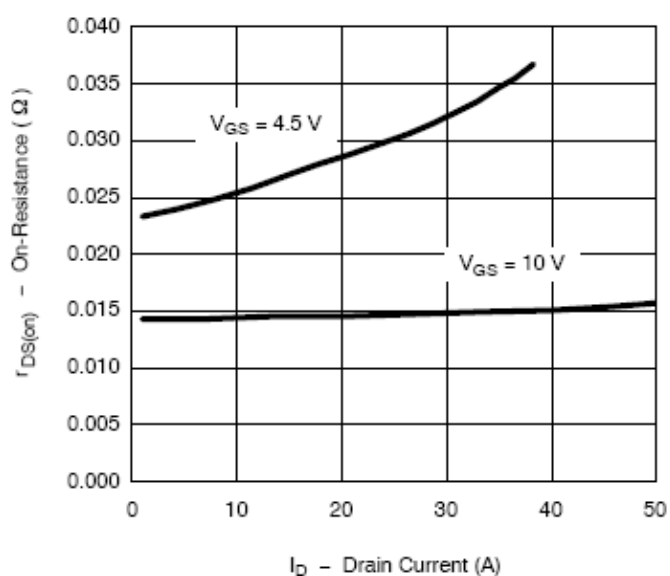
Output Characteristics



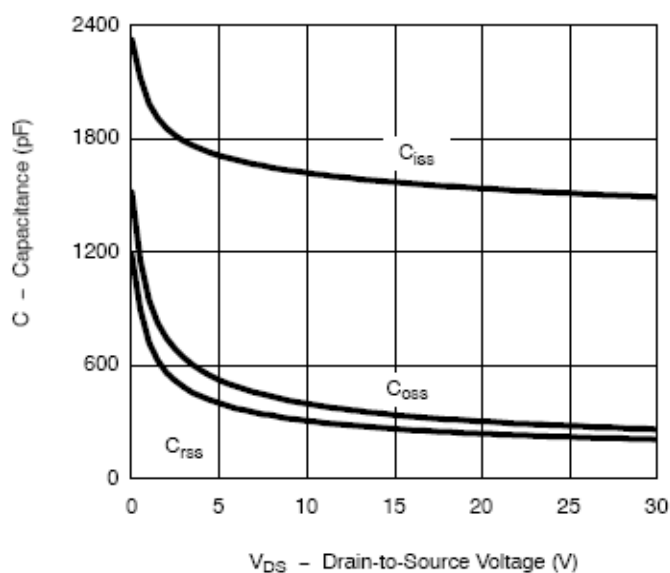
Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance

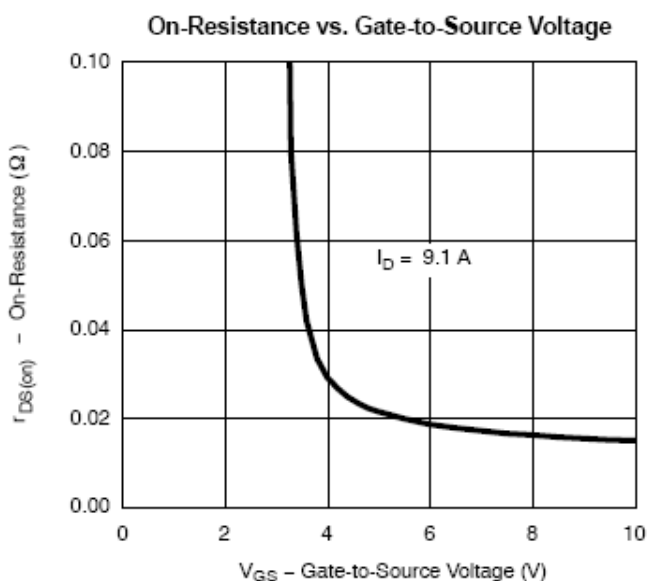
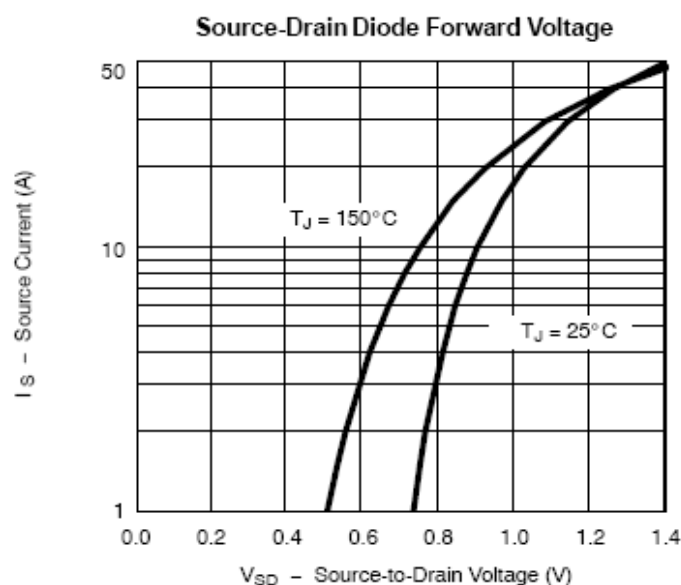
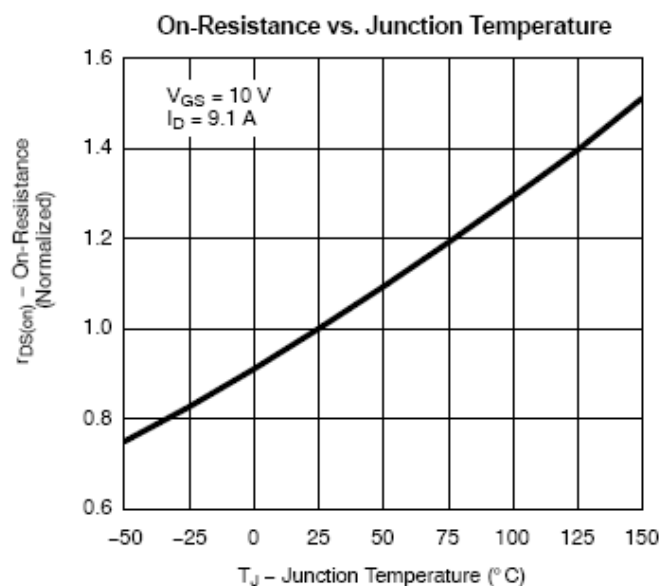
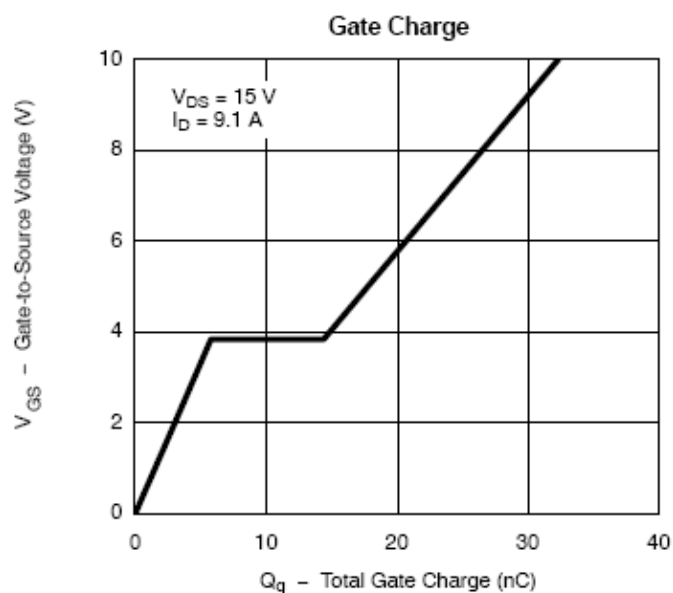




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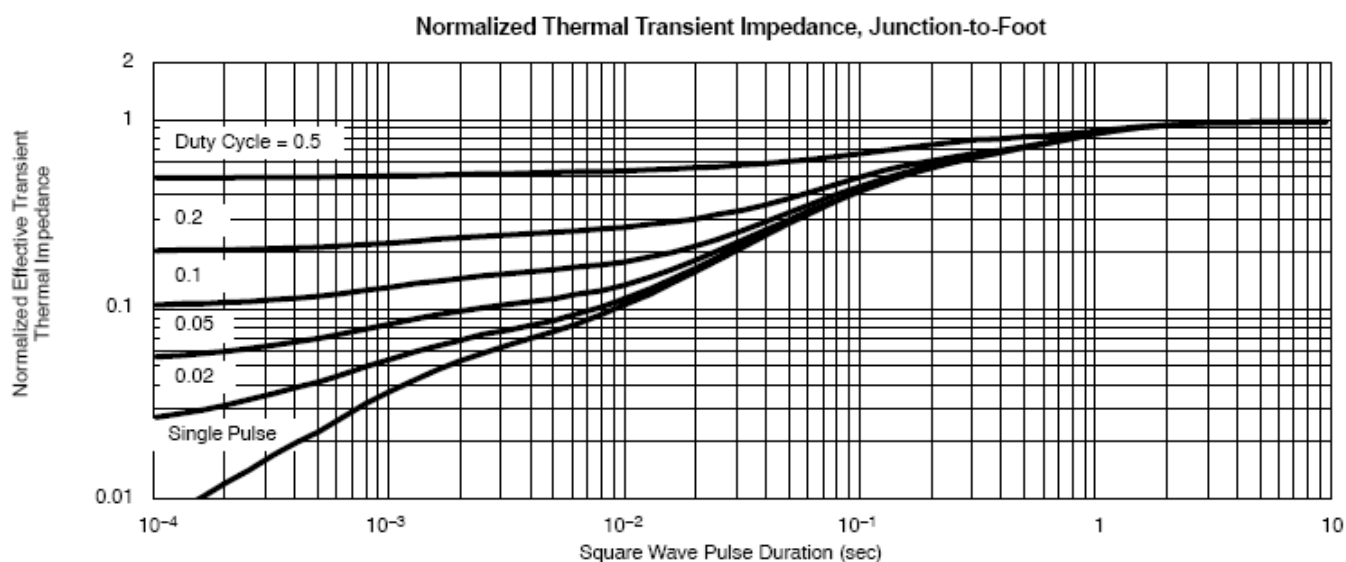
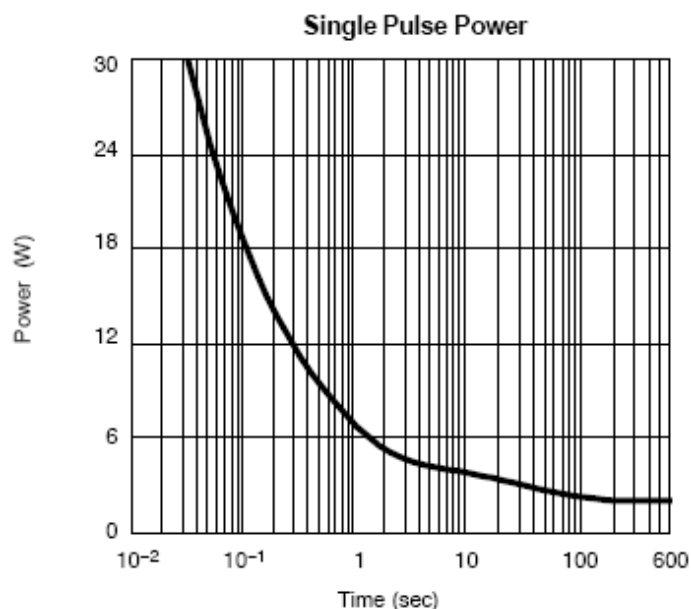
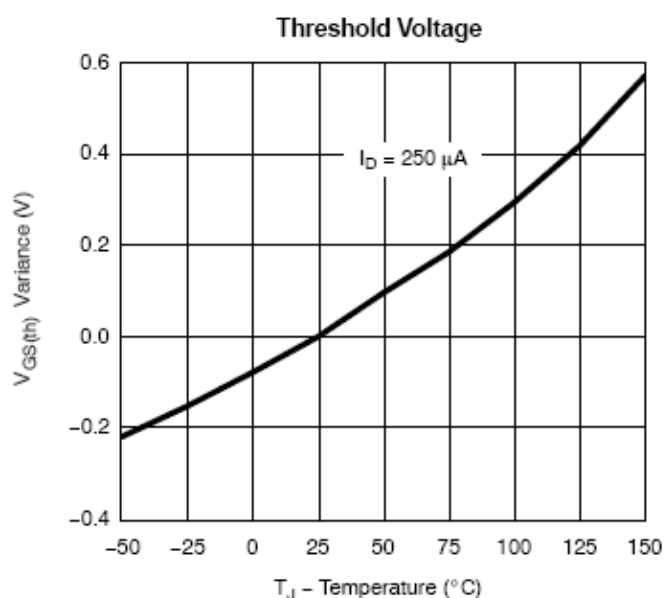




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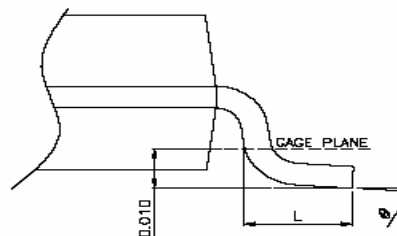
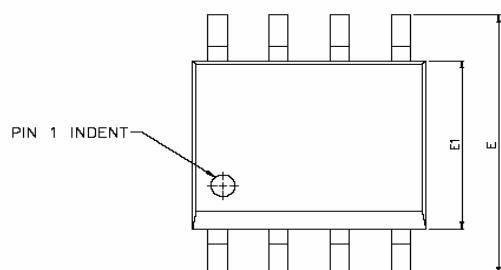




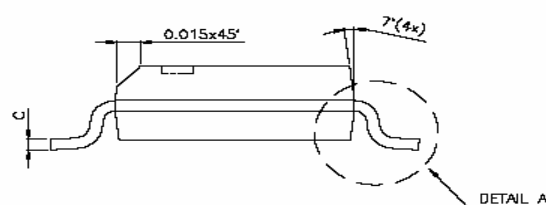
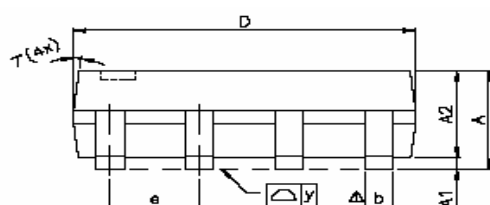
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SOP- 8 PACKAGE OUTLINE



DETAIL A



DETAIL A

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°



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