INTEGRATED CIRCUITS

DATA SHEET

TDA8356
DC-coupled vertical deflection circuit

Product specification
Supersedes data of 1998 Sep 07
File under Integrated Circuits, IC02

1999 Sep 27

Philips Semiconductors

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DC-coupled vertical deflection circuit TDA8356

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - Short-circuit of the output pins (7 and 4)
  - Short-circuit of the output pins to V_P.
- Temperature protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8356 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage	9	14.5	25	V
I_q	quiescent supply current	–	30	–	mA
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	–	–	2	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)	–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)	–	1.5	1.8	V
Flyback switch					
I_M	peak output current	–	–	±1	A
V_{FB}	flyback supply voltage	–	–	50	V
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature	–55	–	+150	°C
T_{amb}	operating ambient temperature	–25	–	+75	°C
T_{vj}	virtual junction temperature	–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8356	SIL9P	plastic single in-line power package; 9 leads	SOT131-2

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BLOCK DIAGRAM

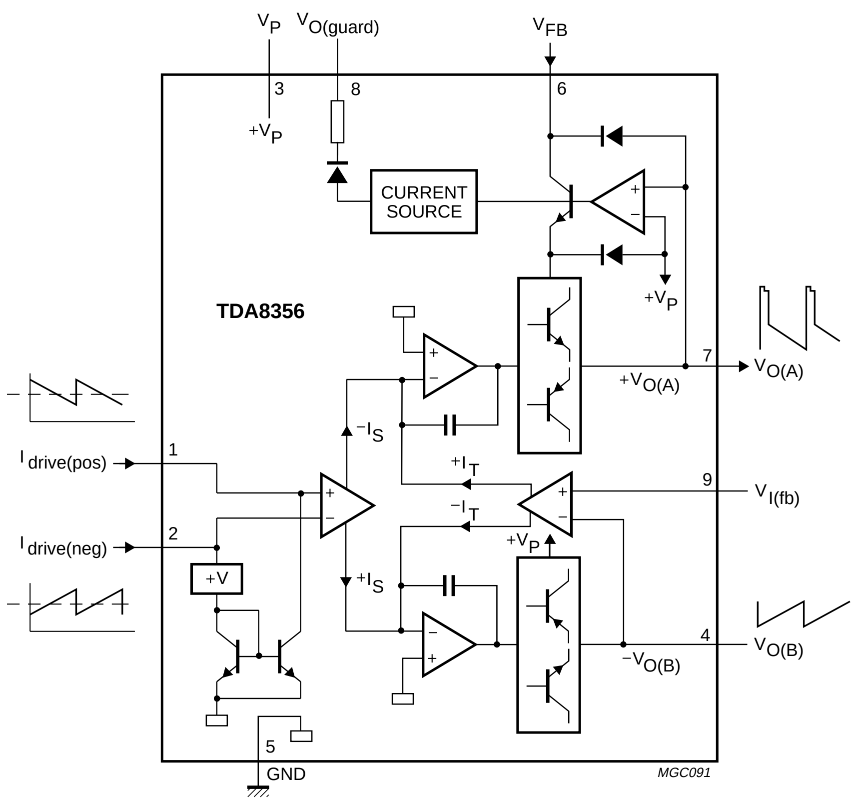

Fig.1 Block diagram.

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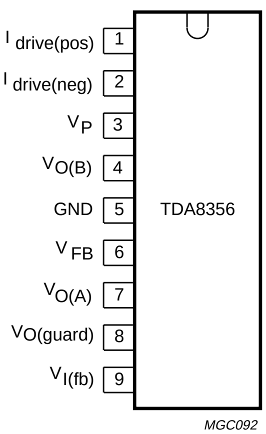
PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



Metal block connected to substrate pin 5.
Metal on back.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in opposite phase. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 2 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). Built-in protections are:

- Thermal protection
- Short-circuit protection of the output pins (pins 4 and 7)
- Short-circuit protection of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- During flyback
- During short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to V_P or ground
- During open loop
- When the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 1	–	2	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
t_{sc}	short-circuiting time	note 2	–	1	hr

Notes

1. I_O maximum determined by current protection.
2. Up to V_P = 18 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ vj-c}$	thermal resistance v_j-case		4	K/W
$R_{th\ vj-a}$	thermal resistance v_j-ambient	in free air	40	K/W

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CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; V_{FB} = 45 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 μA; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9.0	14.5	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 2 A (p-p)	13.2	–	–	V
LE	linearity error	I_O = 2 A (p-p); note 1	–	1	4	%
		I_O = 50 mA (p-p); note 1	–	1	4	%
V_O	output voltage swing (flyback); $V_{O(A)} - V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1 A	–	40	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)} - V_{FB}$)	I_O = –1 A; I_{diff} = 0.3 mA	–	–	1.5	V
$\lvert I_{os} \rvert$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	40	mA
$\lvert V_{os} \rvert$	offset voltage at the input of the feedback amplifier ($V_{I(fb)} - V_{O(B)}$)	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	24	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0	–	–	72	μV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 2	–	6.5	–	V
G_{vo}	open-loop voltage gain $\left(\frac{V_{7-4}}{V_{1-2}}\right)$	notes 3 and 4	–	80	–	dB
	open loop voltage gain $\left(\frac{V_{7-4}}{V_{9-4}}; V_{1-2} = 0\right)$	note 3	–	80	–	dB
V_R	voltage ratio $\frac{V_{1-2}}{V_{9-4}}$		–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop; note 5	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
ΔG_cT	current gain drift as a function of temperature		–	–	10^{-4}	K
$I_{I(sb)}$	signal bias current		50	400	500	μA
I_{FB}	flyback supply current	during scan	–	–	100	μA
PSRR	power supply ripple rejection	note 6	–	80	–	dB
$V_{I(DC)}$	DC input voltage		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	μA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 μA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	μA
		active; $V_{O(guard)}$ = 3.6 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage on pin 8	I_O = 100 μA	4.6	–	5.5	V
	allowable voltage on pin 8	maximum leakage current = 10 μA;	–	–	40	V

Notes

1. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows: Divide the output signal $I_4 – I_7$ (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and linearity error for not adjacent blocks (LENAB) are given below:

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} \; ; \; LENAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

2. Related to V_P.
3. The V values within formulae relate to voltages at or across relative pin numbers, i.e. V_{7-4}/V_{1-2} = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
4. V_{9-4} AC short-circuited.
5. Frequency response V_{7-4}/V_{9-4} is equal to frequency response V_{7-4}/V_{1-2}.
6. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.

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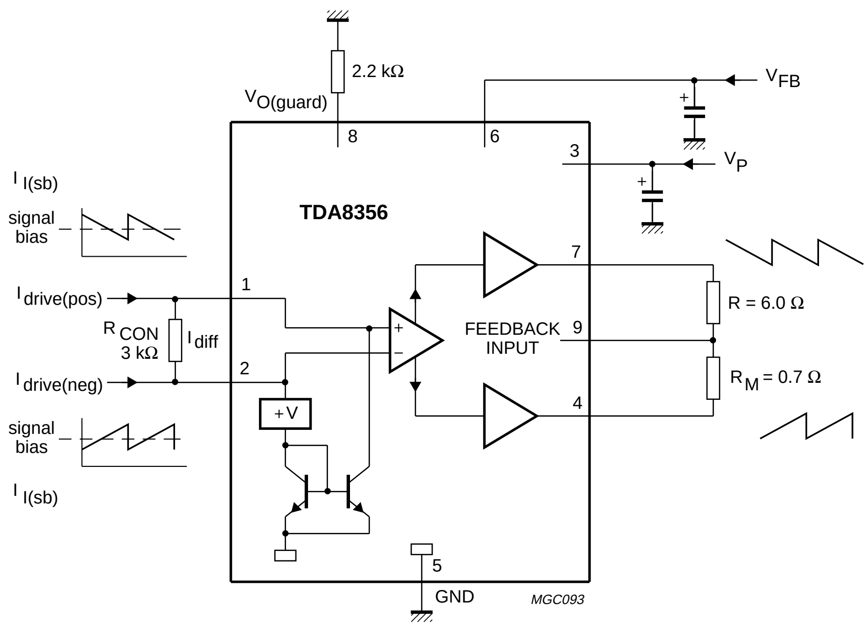

Fig.3 Test diagram.

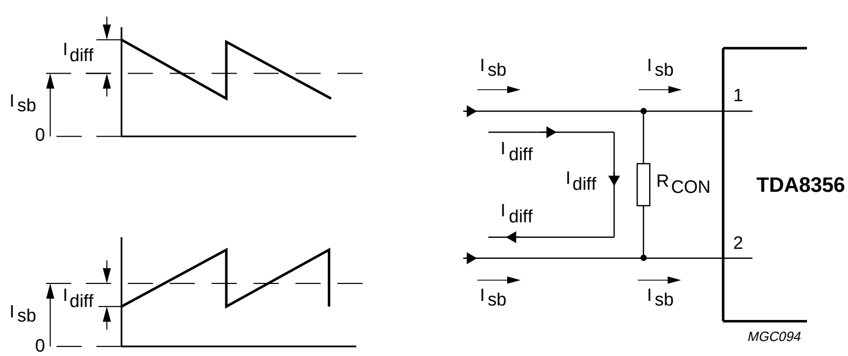

Fig.4 Input currents.

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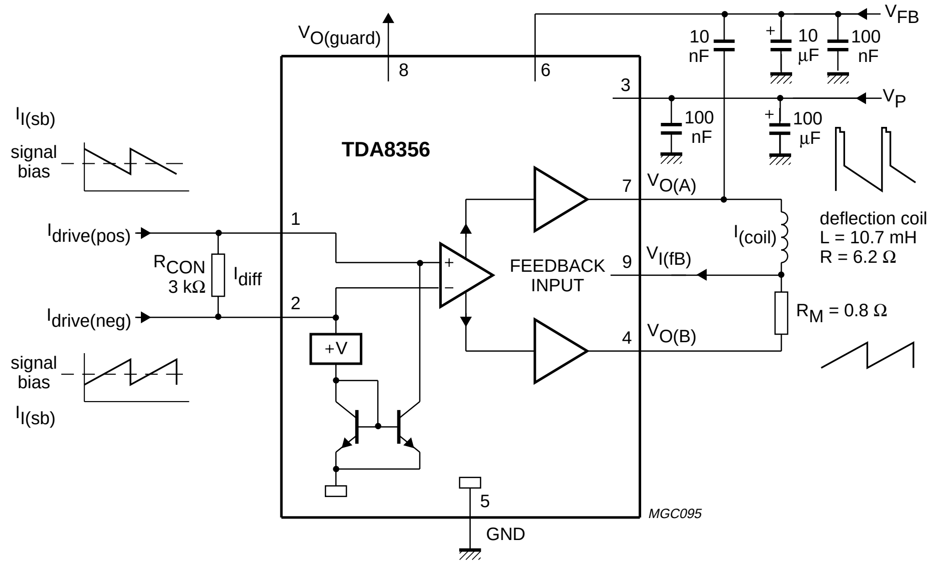
APPLICATION INFORMATION



V_P = 13.5 V; $I_{O(p-p)}$ = 1.87 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p-p)}$ = 500 µA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.5 Application diagram.

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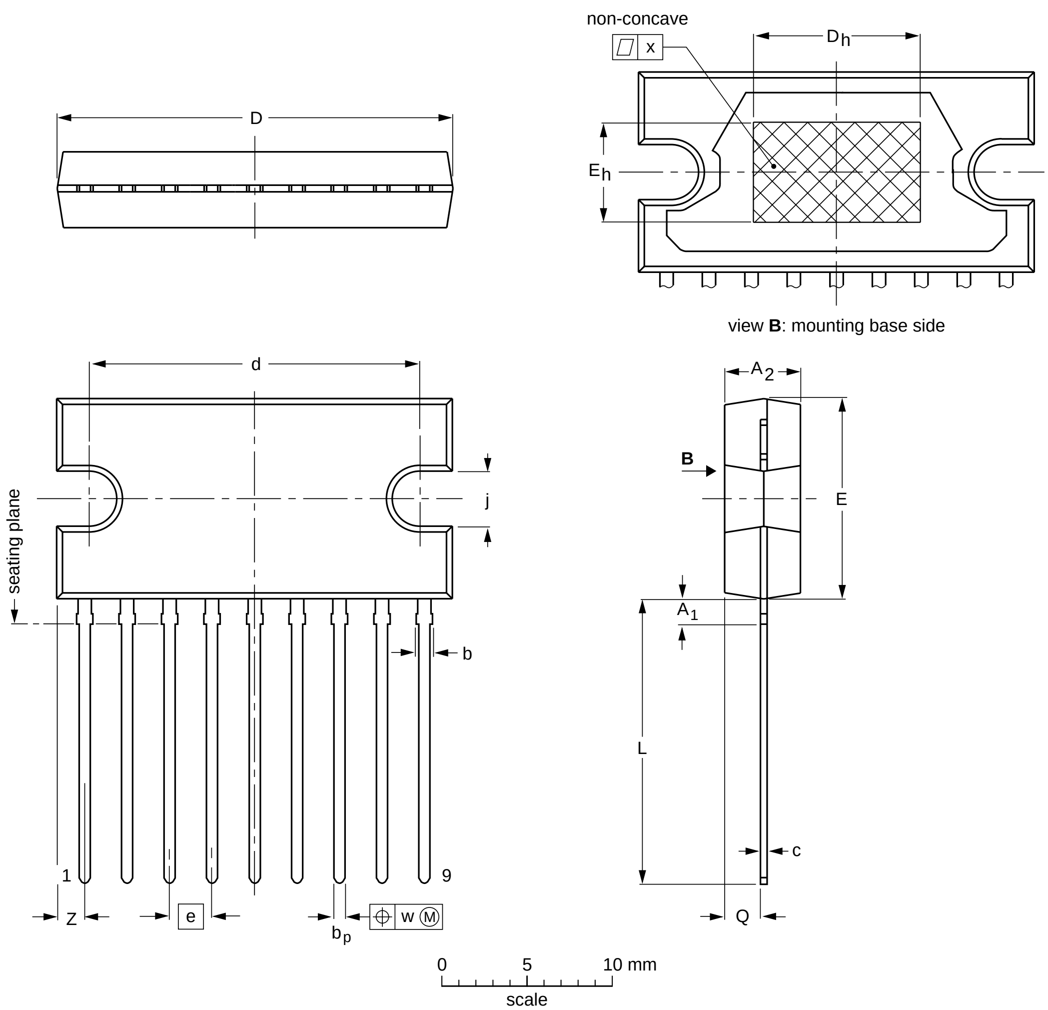
PACKAGE OUTLINE

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A_1 max.	A_2	b max.	b_p	c	D(1)	d	D_h	E(1)	e	E_h	j	L	Q	w	x	Z(1)
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Argentina: see South America
Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140, Tel. +61 2 9704 8141, Fax. +61 2 9704 8139
Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210
Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773
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Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 800 943 0087
China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700
Colombia: see South America
Czech Republic: see Austria
Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905
Finland: Sinikallontie 3, FIN-02630 ESPOO, Tel. +358 9 615 800, Fax. +358 9 6158 0920
France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 4099 6161, Fax. +33 1 4099 6427
Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300
Hungary: see Austria
India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966
Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080
Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200
Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007
Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI), Tel. +39 039 203 6838, Fax +39 039 203 6800
Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057
Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415
Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880
Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087
Middle East: see Italy
Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399
New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811
Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341
Pakistan: see Singapore
Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474
Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW, Tel. +48 22 5710 000, Fax. +48 22 5710 001
Portugal: see Spain
Romania: see Italy
Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919
Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500
Slovakia: see Austria
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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 58088 Newville 2114, Tel. +27 11 471 5401, Fax. +27 11 471 5398
South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382
Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107
Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745
Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263
Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874
Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793
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Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461
United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421
United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 800 943 0087
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