P²CCD FILTER COMBINATION FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8452A is a monolithic integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates a video input switch, a luminance delay line with different delay lengths for the 3.58 MHz and the 4.43 MHz TV systems, chrominance trap, a chrominance band-pass filter and clock drivers for the filters which are driven from an internal voltage controlled oscillator (VCO) locked to the 2 x f_{sc} signal. The 2 x f_{sc} signal is obtained from the decoder IC.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 2)		$V_{p(a)}$	10.8	12.0	13.2	V
digital (pin 12)		$V_{p(a)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 2)		$I_{p(a)}$	10	20	28	mA
digital (pin 12)		$I_{p(d)}$	20	45	70	mA
CVBS inputs (pins 14 and 16)						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Luminance output (pin 3)						
output signal (peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns
Bandwidth	at –3 dB	B	3.7	3.8	–	MHz
Chrominance output (pin 5)						
output signal (peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Bandwidth (Fig.3)	at –3 dB	B	–	1.15	–	MHz
CVBS output (pin 4)						
output signal (peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns
Bandwidth (Fig.4)	at –3 dB	B	5.5	6.5	–	MHz
Output resistance		R_O	300	500	800	Ω
Oscillator input signal (peak-to-peak value)		$V_{8(p-p)}$	200	–	–	mV

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).

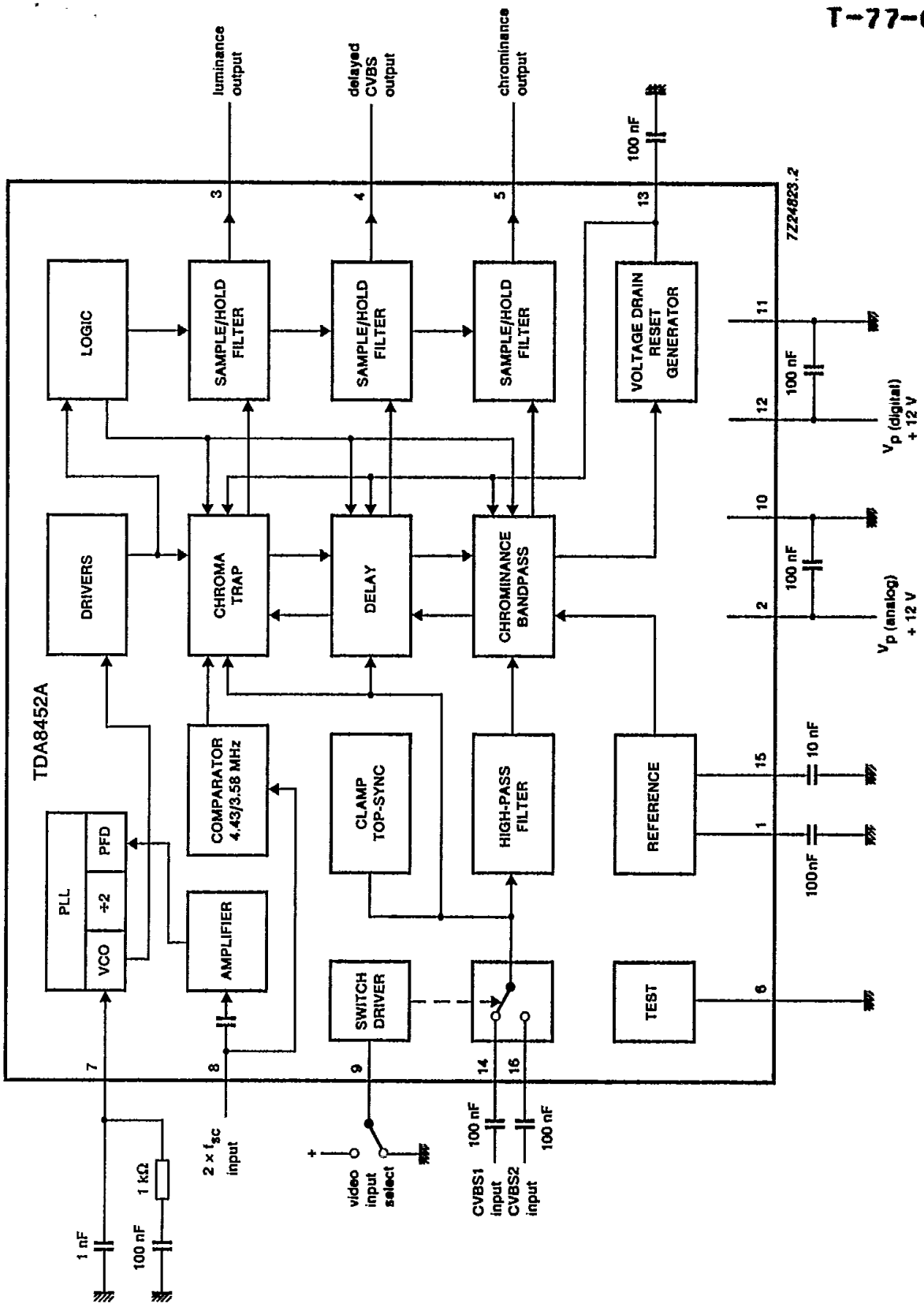

Fig.1 Block diagram.

PINNING

1	Reference decoupling
2	Analog supply voltage input
3	Luminance output
4	Delayed CVBS output
5	Chrominance output
6	Test pin (to be grounded for normal operation)
7	PLL filter
8	2 x f_{sc} input
9	CVBS input select
10	Ground (analog)
11	Ground (digital)
12	Digital supply voltage input
13	Voltage drain reset generator decoupling
14	CVBS1 input
15	Reference decoupling
16	CVBS2 input

FUNCTIONAL DESCRIPTION

T-77-07-13

The composite video signal (CVBS1 and CVBS2) is applied to pin 14 and/or pin 16. The signal is then routed through three separate paths before being applied to the sample-and-hold filter output stages as follows:

- via a delay line with a delay length of 0.62 μs (for the 4.43 MHz TV system) without filter characteristics. The output signal can be used to drive the sync separation circuit, teletext and SECAM decoders etc.
- via a luminance delay line with chrominance trap with a delay length of 2.09 μs (for the 4.43 MHz TV system). For the 3.58 MHz system the luminance signal will 'skip' part of the delay line so that the total delay of the chrominance signal and the luminance signal are the same (inclusive of the decoder delay and the direct delay of the TDA8451A). The decoder IC, TDA8466, detects whether the subcarrier frequency of the input signal is 3.58 or 4.43 MHz and applies it to the TDA8452A via the DC level of the 2 x f_{SC} reference signal.
- via a chrominance bandpass filter with a delay length of 1.02 μs (for the 4.43 MHz TV system).

The outputs from the delay lines and the bandpass filter are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.
The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{SC} signal from its reference oscillator (the amplitude of this signal may be small, min. 200 mV(p-p)). The VCO operates at 4 x f_{SC} and the delay lines are 4 phase clocked at $4f_{SC}$.
The P^2CCD filter combination requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 13. A circuit for the TDA8452A together with PAL decoder (TDA8391) is illustrated in Fig.5.
A circuit for the TDA8452A together with PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.6. The TDA8490 can also be used in combination with the TDA8391.
Figures 7 and 8 illustrate the luminance and CVBS channel response on T and 2T pulse.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_p(a)$	–	13.2	V
Supply voltage (digital)		$V_p(d)$	–	13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$		55	K/W

QUALITY SPECIFICATION

Quality level according to URV-4-2-59/601
(except for pins 14 and 15; 700 V; Human body model)

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified (note 1).

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 2) analog		$V_p(a)$	10.8	12.0	13.2	V
Supply current (pin 2) analog		$I_p(a)$	10	20	28	mA
Supply voltage (pin 2) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Supply voltage (pin 12) digital		$V_p(d)$	10.8	12.0	13.2	V
Supply current (pin 12) digital		$I_p(d)$	20	45	70	mA
Supply voltage (pin 12) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Total power dissipation		P_{tot}	–	0.78	–	W
Composite video inputs (pins 14 and 16)						
AC coupled and clamped to top sync						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Input current (non-selected input)		I_I	–	–	0.1	μA
Input current during non-clamping period of selected input		I_I	1.0	3.0	5.0	μA
Input capacitance		C_I	–	5	–	pF
Crosstalk between selected/non-selected channels	R_I = 75 Ω					
at f_{sc} = 1.5 MHz		α	60	65	–	dB
at f_{sc} = 5.0 MHz		α	–	50	–	dB
Video switch control (pin 9)						
Video input (pin 14)		V_9	0	–	1.5	V
Video input (pin 16)		V_9	4	–	V_p	V
Oscillator input signal (pin 8)						
Input signal (peak-to-peak value)	2 x f_{sc}	$V_{8(p-p)}$	200	–	–	mV
Input capacitance		C_I	–	6	–	pF
Input resistance		R_I	–	80	–	kΩ
Input voltage for 3.58 MHz TV system		V_8	6.7	–	V_p	V
4.43 MHz TV system		V_8	0	–	5.3	V

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance signal output (pin 3)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	0.23	0.32	0.46	V
Output resistance		R_0	300	500	800	Ω
Output level for top sync		V_3	3.0	–	7.0	V
Luminance output internal load		I_3	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{3(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{3(rms)}$	–	–	4	mV
at 17.73 MHz		$V_{3(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity black-to-white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.95	–	–	
Linearity black-to-white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.94	–	–	
Bandwidth	at –3 dB	B	3.7	3.8	–	MHz
Frequency response with regard to 0 MHz (Fig.2)						
at 2.2 MHz		Δf	–1.0	0.5	2.0	dB
at 3.0 MHz		Δf	–0.5	1.0	2.5	dB
at 3.8 MHz		Δf	–4.0	–2.5	–1.0	dB
at 4.26 MHz		Δf	–19	–16	–10	dB
at 4.43 MHz		Δf	–	–25	–20	dB
at 4.64 MHz		Δf	–19	–12	–10	dB
at 5.5 MHz		Δf	–5.0	–2.5	0	dB
T and 2T response (Fig.7) (CVBS input signal = 0.6 V peak-to-peak value)						
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance signal output (pin 5)						
Output signal (chrominance input signal = 0.465 V peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Output resistance		R_0	300	500	800	Ω
DC output level		V_5	3.0	–	7.5	V
Internal load of chrominance output		I_5	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{5(rms)}$	–	–	0.2	mV
at 8.87 MHz		$V_{5(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{5(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity of output signals	note 4					
input = 0.45 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.97	–	
input = 0.65 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.95	–	
Bandwidth (Fig.3)	at –3 dB	B	–	1.15	–	MHz
Frequency response with regard to the top at 4.43 MHz (Fig.3)						
at 0.9 MHz		Δf	–	–22	–17	dB
at 1.9 MHz		Δf	–	–35	–30	dB
at 2.5 MHz		Δf	–	–30	–25	dB
at 3.0 MHz		Δf	–	–20	–16	dB
at 3.8 MHz		Δf	–3.5	–2.5	–1.5	dB
at 4.93 MHz		Δf	–4.0	–3.0	–2.0	dB
at 5.6 MHz		Δf	–	–20	–16	dB
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Delayed signal output (pin 4)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	0.49	0.70	0.98	V
Output resistance		R_0	300	500	800	Ω
Internal load of delayed output		I_4	0.4	–	1.5	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Output sync pulse (input sync pulse = 210 mV peak-to-peak value)		$V_{4(p-p)}$	210	–	–	mV
Output level for top sync		V_4	2.5	–	6.5	V
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{4(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{4(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{4(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	65	70	–	dB
Linearity black to white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.95	–	–	
Linearity black to white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.94	–	–	
Bandwidth (Fig.4)	at –3 dB	B	5.5	6.5	–	MHz
Frequency response with regard to 2.2 MHz (Fig.4)						
at 0.0 MHz		Δf	–2.5	–1.5	–0.5	dB
at 0.9 MHz		Δf	–2	–1	–0	dB
at at 3.1 MHz		Δf	0	1.0	1.5	dB
at 5.5 MHz		Δf	–3	–1	+0.5	dB
T and 2T response is given in Fig.7 (CVBS input signal = 0.6 V peak-to-peak value)						
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns

Notes to the characteristics

1. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V (peak-to-peak value); 100% contrast; 75% saturation.
   In this condition the input signal is formed by the following components:
   210 mV(p-p) sync pulse
   490 mV(p-p) black-to-white
   465 mV(p-p) chrominance
2. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) connected directly to pins 1 and 3, pins 1 and 4 or pins 1 and 5.
3. The signal-to-noise ratio is specified as: nominal $V_{out(p-p)}/V_{noise(rms)}$ (0-5 MHz) at a CVBS input signal specified in note 1.
4. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

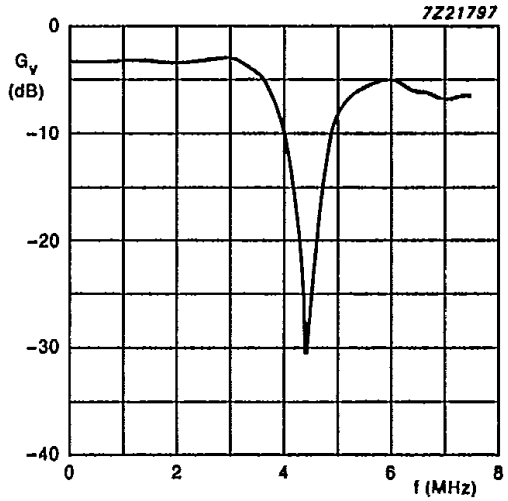

Fig.2 Typical frequency response of luminance signal.

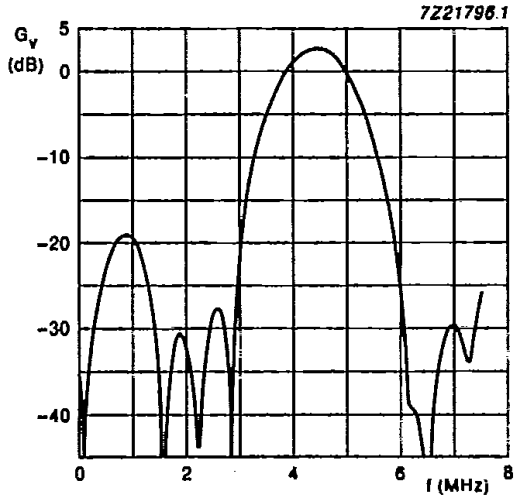

Fig.3 Typical frequency response of chrominance signal.

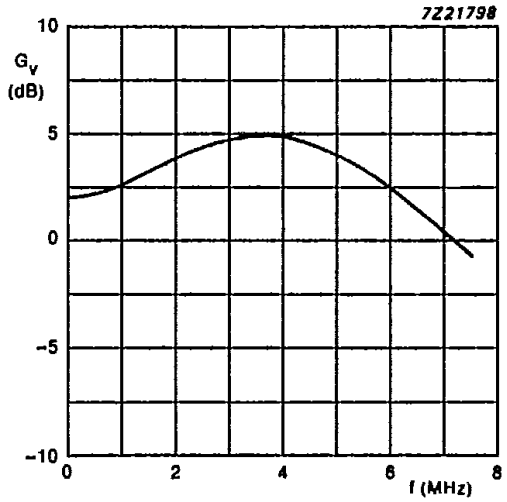

Fig.4 Typical frequency response of delayed signal.

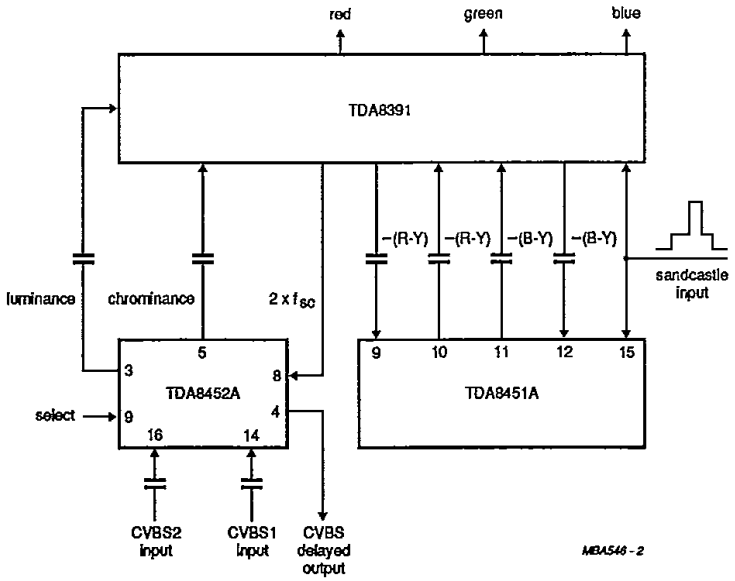

Fig.5 PAL decoder configuration.

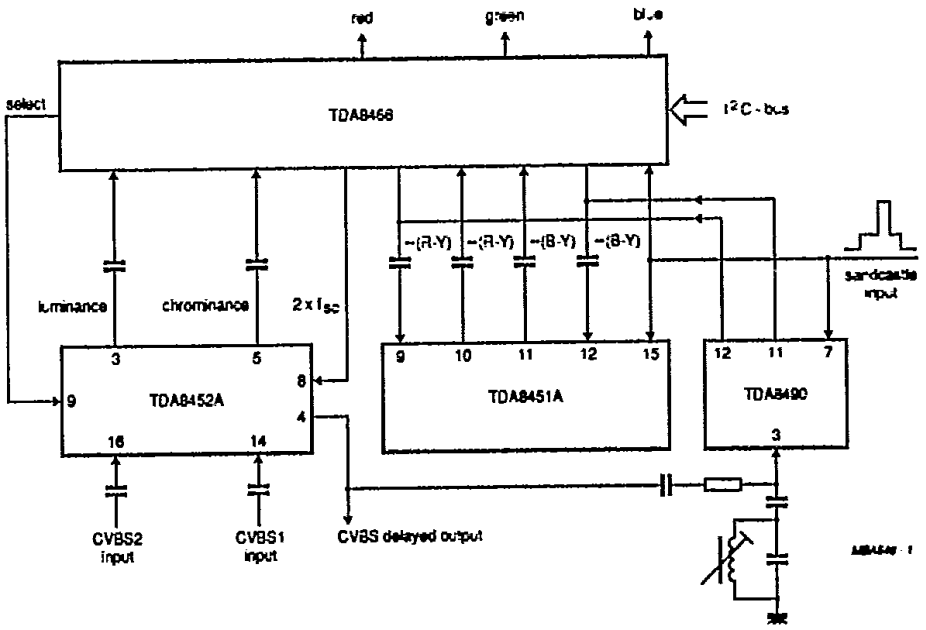

Fig.6 PAL-NTSC-SECAM decoder configuration.

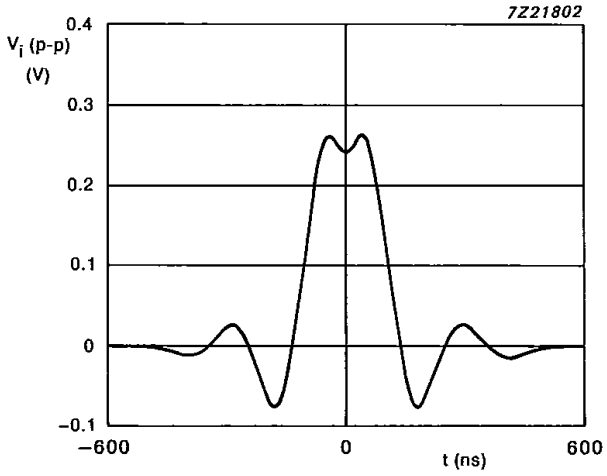

Fig.7(a) Luminance response (T pulse).

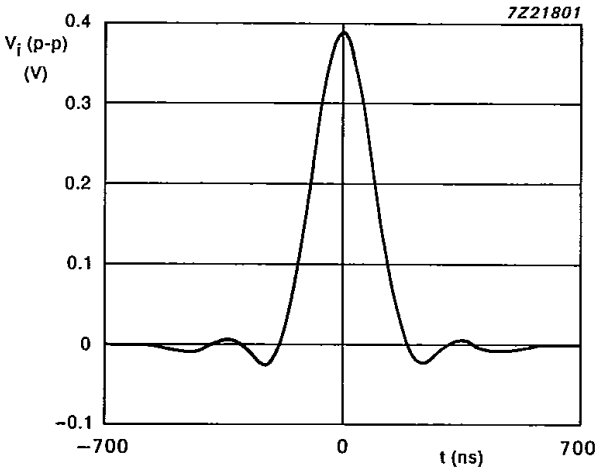

Fig.7(b) Luminance response (2T pulse).

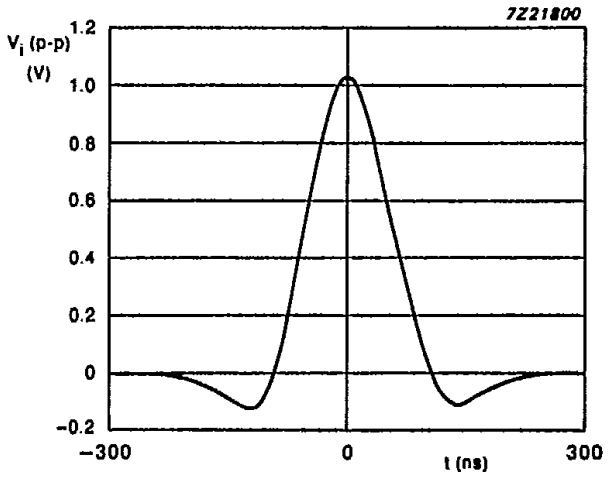

Fig.8(a) CVBS channel response (T pulse).

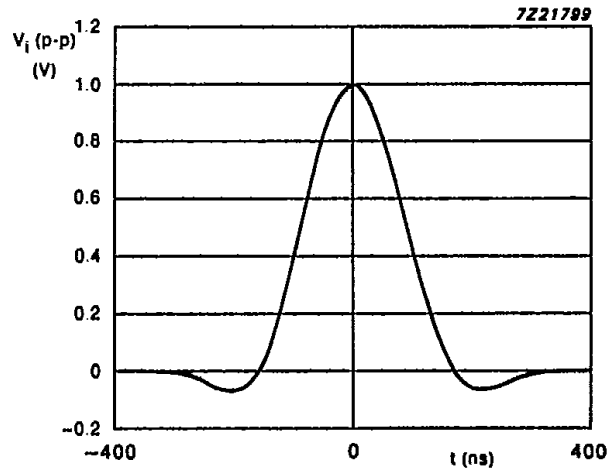

Fig.8(b) CVBS channel response (2T pulse).