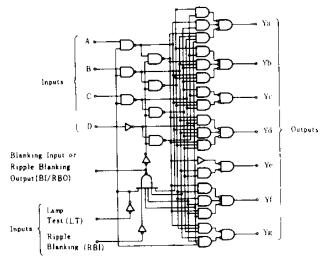
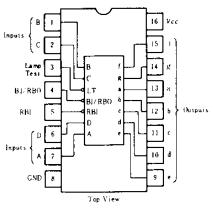
# HD74LS48 • BCD-to-Seven-Segment Decoder 'Driver (Internal Pull-up outputs)

The HD74LS48 features active high outputs for driving lamp buffers. This circuit has full ripple blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. It contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

#### BLOCK DIAGRAM



## PIN ARRANGEMENT



#### **RECOMMENDED OPERATING CONDITIONS**

Item	S	ymbol	min	typ	max	Unit	
High level		a-g			100	μA	
output current	Іон	BI/RBO	•		- 50	μA	
Low level	1.	a∼g	····		6	mА	
output current	IOL	BI/RBO			3.2	mА	

#### **FUNCTION TABLE**

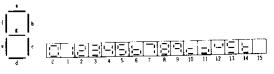
Decimal or			Inc	uts							Outputs				: ⊣Note
Function	LT	RBI		C	В	A	BLRBO	a	<u>ь</u>	с – с	d	e	f	g	None
0	<u>н</u>	н	L	L	L	L	н	H	н	н	н	н	н	L	Ţ
	н		L.	+ <u>-</u>	L	H	+ н т		Н	H .	Ĺ	L.	I.	L	
	— <u>н</u> —	$+\hat{x}$	L		H	L	H	H	Н	L.	н	н	L	н	_
3	н	+ <u>×</u> ···	<u></u>	• <u>-</u>	н	н	н	н	т н	н	н	L	L	н	-
	H	×	L	н	L	L	н	Ľ.	н	н	L	L	н	Н	
5	H H	× ····	 L	н	L.	н	H	н	1.	н	н	L_	н	н	
	н.	- <u>- ×</u>	L	Н	Н	L	<u>н</u>	L	L	н	н	<u> </u>	н	н	-
	н -		·	↓ H	н	H	н	н	н	н	L	L	L	L	- 1
8	H	×	н	1	L.	L	н	н	н	Н	н	н	<u> </u>	H	-
	H H	- <del>x</del>	н	L	L	н	н	Н	н	і н	L	L	<u> </u>	н	_
10	<u> </u>	× · · · · ·	н	L	н	L	H I	L.	L	L	н	н	L	н	
10	H		Н	L	Н	н	н	Ľ. –	Į.,	н	Н	L	I.	н	4
11	H	×	н	H	L	L	н	L	н	1.	L	L	H	н	-
12	н	+ <del>x</del>	н	н	L	н	н	Н	L	L	н	L	н	н	
13	<u>н</u>	$+-\frac{2}{x}$	н н	н	Н	+	н	L	L	L	Н	н	н	н	4
15	н	+ <del>· ×</del> · -	- H	н	н	н	H H	L	L	L	L	L	L	L	
BI	×	×	×		×	×	L	L	L	1.	L.	L	L	<u> </u>	2
	<u> </u>	∔ ;	L L	- <u>î</u>	L	 L	L	L	L.	L	L	L	L	L	3
RBI		• <u> </u>	• <u>-</u>	+	×	<u>-</u>	<u>н</u>	<u>н</u> –	Н Н	н	н	Н	<u> </u>	н	4
LT		1	i										1.1.1		

#### H; high level, L; low level, X; irrelevant

- Notes: 1. The blanking input (B1) must be open or held at a high logic level when output functions 0 through 15 are desired.
  - When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
  - 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO)

goes to a low level (response condition).

4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.



Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		Vin			2.0	-	-	V
		VIL			-	_	0.8	۷
	a-g BI/RBO	Voн	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$\frac{I_{OH} = -100 \mu A}{I_{OH} = -50 \mu A}$	2.4			V
				$I_{OL} = 2mA$	-	_	0.4	
Output voltage	a∼g	Vol		$I_{OL} = 6 \text{mA}$			0.5	v
	BI/RBO		$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}$	<i>IoL</i> =1.6mA		_	0.4	v
				$I_{OL} = 3.2 \text{mA}$			0.5	
Output current * *	a~g	Іо	$V_{CC} = 4.75 V, V_O = 0.85 V$		-1.3			mА
	except	Ін	$V_{CC} = 5.25 \text{V},  V_I = 2.7 \text{V}$		-	-	20	μA
_	BI/RBO	_	$V_{cc} = 5.25 V, V_{l} = 0.4 V$		-	-	-0.4	
Input current	BI/RBO	hι	$V_{cc} = 5.25 V, V_l = 0.4 V$			_	-1.2	mA
	except BI/RBO	Ī.	$V_{cc} = 5.25 \text{V},  V_l = 7 \text{V}$				0.1	mA
Short-circuit output current	BI/RBO	los	$V_{CC} = 5.25 V$		-0.3	-	-2	mА
Supply current **	*	lcc	$V_{cc} = 5.25V$	.,	-	25	38	mA
Input clamp voltage		Vik	$V_{CC} = 4.75 \text{V}, \ I_{IN} = -18 \text{mA}$		_		-1.5	v

# **ELECTRICAL CHARACTERISTICS** ( $Ta = -20 \sim +75^{\circ}C$ )

\* V<sub>CC</sub>=5V, Ta=25°C

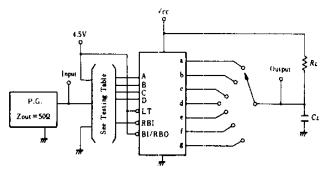
\*\* Input condition as for  $V_{OH}$ \*\*\*  $I_{CC}$  is measured with all outputs open and all inputs at 4.5V.

## **SWITCHING CHARACTERISTICS** ( $V_{CC} = 5V$ , $T_a = 25^{\circ}C$ )

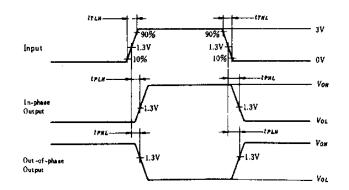
Item	Symbol	Input	Test Conditions	min	typ	max	Unit
	tphl.		$c = 15$ , E $p_{\rm c} = 4k0$		+	100	
<b>.</b>	t <i>PLH</i>	A	$C_L = 15 \mathrm{pF},  R_L = 4 \mathrm{k} \Omega$	-	-	100	ns
Propagation delay time	tPHL.	DDT	c = 15 E D = 610		—	100	
	tPLH .	RBI	$C_L = 15 \mathrm{pF}, R_L = 6 \mathrm{k} \Omega$	_		100	ns

# **TESTING METHOD**

1) Test Circuit



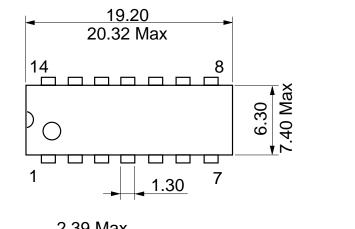
#### Waveform

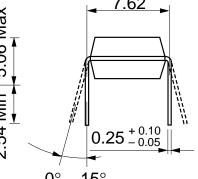


#### 2) Testing Table

1			Inputs	•				(	Dutput	s		
ltem	RBI	D	C	B	A	a	b	с	d	e	f	g
	4.5V	GND	GND	GND	IN	OUT	-	_	0UT	OUT	OUT	
tp_LH	4.5V	GND	GND	4.5V	IN			OUT	-	OUT	-	
<b>t</b> PHL	4.5V	GND	4.5V	4,5V	IN	OUT	OUT		OUT	OUT	OUT	OUT
	IN	GND	GND	GND	GND	OUT	TUO	OUT	OUT	OUT	OUT	

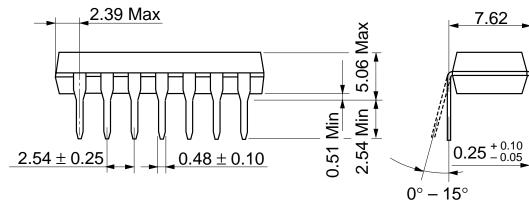
Unit: mm





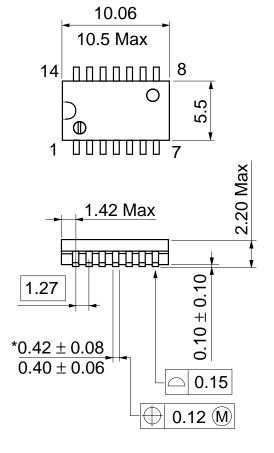
AAAA

Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

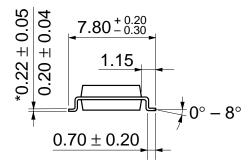


Unit: mm





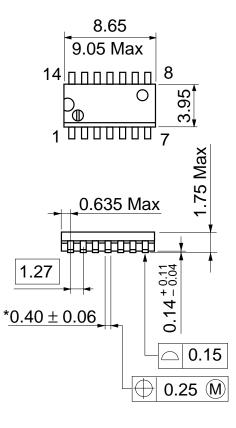
\*Dimension including the plating thickness Base material dimension



Hitachi Code	FP-14DA
JEDEC	
EIAJ	Conforms
Weight (reference value)	0.23 g

Unit: mm



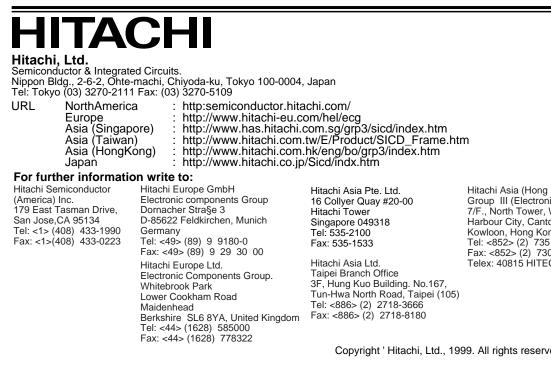


Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

\*Pd plating

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