TV Encoder

GENERAL DESCRIPTION

CS8552 provides full conversion from digital video format YCbCr into NTSC/PAL composite and S-video. It can be used in VCD, DVD, digital VCR application.

Two-times oversampling reduces the output filter requirements and guarantees no alias interference by internal UV filters and Y filter.

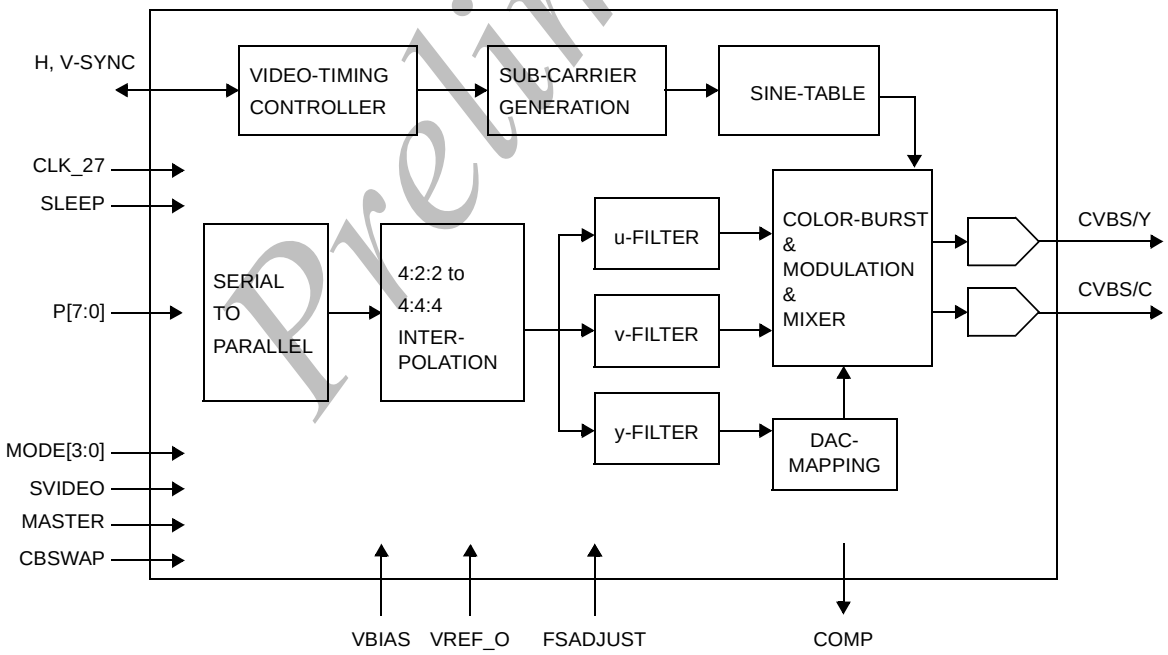
Two 9-bit DACs provides two channels for a S-video output port or two composite video outputs with high quality of image.

32-pin package and pin assignment make CS8552 compatible with major vendors.

FEATURES

- Designed special for VCD, Karaoke, digital VCR, DVD, DIGITAL set-top box.
- Support the following 4 modes: NTSC, PAL-M, PAL-BDGHI, PAL-Nc
- 8-bit 4:2:2 YcbCr inputs for glueless interface to MPEG decoders
- CVBS (composite YC) or S-video (Y and C) outputs
- Support CCIR-6-1 for mat, non-square pixel
- 2x oversampling simplify external filtering
- 6MHz and 1.3MHz anti-alias filters for Y and U/V channels each
- On-chip color bar generation
- 2 channels of 9-bit DAC
- Support master and slave modes
- Support interlace operation only
- Automatic mode detection/switching in slave mode
- 3.3V supply voltage; 5V tolerant for all digital I/O pins

BLOCK DIAGRAM



Century Semiconductor, Inc.
Taiwan:
No. 2, Industry East Rd. 3rd,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

USA:
1485 Saratoga Ave. #200
San Jose, CA, 95129
Tel: 408-973-8388 Fax: 408-973-9388

Sales@century-semi.com
Sales@century-semi.com.tw
www.century-semi.com

PIN CONNECTION DIAGRAM

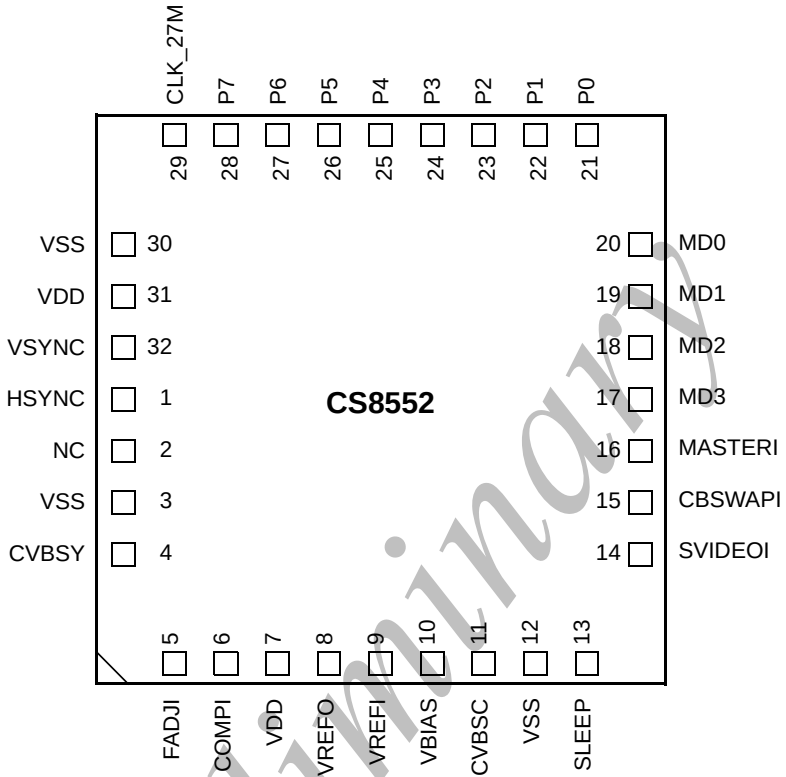


Figure-1 32-pin PLCC

PIN DESCRIPTION

Name	I/O	Pin	Description
CLKI	I	29	Pixel clock, 27MHz, twice the Y sample rate
VSYNC	I/O	32	Vertical sync, output in master mode or input in slave mode, is synchronized by CLK.
HSYNC	I/O	1	Horizontal sync, output in master mode or input in slave mode, is synchronized by CLK too.
P[7:0]	I	28-21	YCbCr pixel inputs (TTL compatible). Also, synchronized by CLK with respect to the incoming HSYNC timing, the higher index corresponds to a greater significance.
MD[3:0]	I	17-20	Configuration inputs
MASTER	I	16	in 0: slave mode, h and v sync are inputs. 1: master mode, h and v sync are outputs.
CBSWAP	I	15	0: normal Cr, Cb sequence. 1: swaps Cr, Cb sequence
SVIDEO	I	14	0: composite output same signal on both Y, C channels, 1: s-video output, Y, C channels.
SLEEP	I	13	1: power down, reset 0: normal operation
FSADJUST	I	5	Full scale adjust control pin. A resistor is connected to GND. Used to control the full-scale output current on analog outputs.
COMP	I	6	Compensation pin. A 0.1μF capacitor is used to bypass this pin to VCC.
VREFO	I	8	Voltage reference output, typically 1.2V, may be used to connect to VREFI input.
VREFI/VRDAC	I	9	Voltage reference input, typically 1.235V. A 0.11μF capacitor must be used to decouple this input to GND. DAC current switch reference input, connect to VREFO output.
VBIAS	O	10	DAC bias voltage, 0.7 v less than COMP signal
CVBS/C	O	11	Composite output or chrominance
CVBS/Y	O	4	Composite output or luminance (with blanking and sync)
VAA		7	Analog power
VDD		31	Digital power
GND		30	Digital ground
AGND		3, 12	Analog ground
NC		2	No connection

FUNCTIONAL DESCRIPTION

MODE configuration

See**Table 1** to **Table 3** for details.

master = 1: master mode

horizontal sync and vertical sync are generated from internal timing and are output at the rising edge of clk_27.

md[3]: define EFIELD function
- 0: vsync is output pin
- 1: vsync is even/odd field indicator, vsync=0 even, vsync=1 odd.

md[2]: define PAL625 function
- 0: 525 line operation is set.
- 1: 626 line operation is set.

master = 0: slave mode

Horizontal sync and vertical sync are inputs that are synchronized by clk_27.

A falling edge of VSYNC* occurring within ±1/4 of a scan line from the falling edge of HSYNC* cycle time indicates the beginning of Field-1. A falling edge of VSYNC* occurring within ±1/4 of a scan line from the middle point of the line indicates the beginning of Field-2. See **Figure 2**

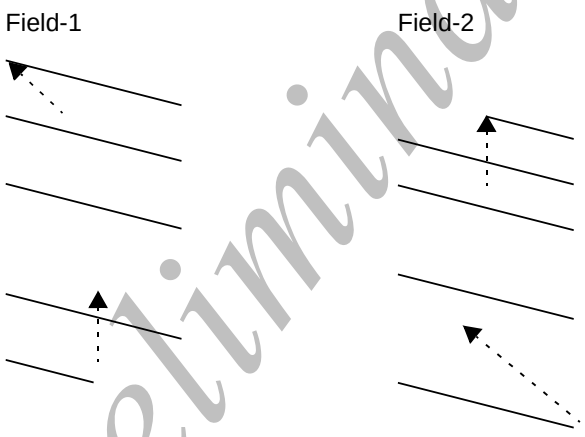


Figure-2

md[3]: define YCSWAP
- 0: normal operation.
- 1: Swap the luma and chroma samples.

md[2]: define SETUP function
- 0: 7.5 IRE setup is enabled for NTSC and PAL-M, with scaling for 92.5% black-to-white range, other PALs with normal 100% black-to-white range.
- 1: 7.5 IRE setup is disabled for NTSC and PAL-M, with scaling for 100% black-to-white range.

md[1]: define PALSA function, South America.
- 0: Normal operation.
- 1: PAL-M used for Brazil 525 lines operation. PAL-Nc used for Argentina 625 lines operation.

Table-1

Mode	Mode[3]	Mode[2]	Mode[1]	Mode[0]
Slave	YCSWAP	SETUP	PALSA	RESERVED
Master	EFIELD	PAL625	RESERVED	RESERVED

EFIELD EFIELD is used when configured as a master. When EFIELD is set low, the Normal vsync* signal is output on the VSYNC* pin. When EFIELD is set high, field ID information is output on the VSYNC* pin (VSYNC* low for Field-1 and high for Field-2)

PAL625 PAL625 is used when configured as a master. When PAL625 is set low, 525-line operation is selected. When PAL625 is set high, 625-line operation is selected. This mode is set by automatic detection when configured as a slave.

YCSWAP YCSWAP should normally be set to zero. When configured as a slave, this bit can be set high to swap the luma and chroma samples, thus altering the pixel sequence with respect to the incoming HSYNC* timing reference.

SETUP SETUP is normally low for the common video modes. The setup and scaling function is toggled when this bit is high. When SETUP is low, the 7.5IRE setup is enabled for NTSC and PAL-M with scaling amplified for a 92.5% black-to-white range; other PAL formats have setup disabled with normal 100% scaling. When SETUP is high, the 7.5 IRE setup is disabled for NTSC and PAL-M with 100% black-to-white range scaling; other PAL formats have setup enabled with amplified scaling.

PALSA PALSA is normally low for the common video modes. South American video Standards can be enabled by setting this bit high. For 525-line operation, the PALSA enables PAL-M for Brazil; in 625-line operation, the PALSA enables PAL-Nc for Argentina.

Table-2 Master mode:

master	Mode[3:0]	System	PAL-625	PALSA	Fv Hz	Fh Hz
1	X000 X010	(Normal setup) NTSC	0	0	59.94	15734.26
1	X000 X010	PAL-M	0	1	59.94	15734.26
1	X000 X110	PAL-BDGHI	1	0	50.00	15625
↑ 1	X010 X110	PAL-Nc	1	1	50.00	15625

Table-3 Slave mode:

Master	Mode[3:0]	System	PAL-625	PALSA	Fv hz	Fh Hz
0	X000	NTSC	0	0	59.94	15734.26
0	X010	PAL-M	0	1	59.94	15734.26
0	X000	PAL-BDGHI	1	0	50.00	15625
0	X010	PAL-Nc	1	1	50.00	15625

PIXEL INPUT/OUTPUT TIMING

1. clk is 2x the luminance sampling rate (13.5 MHz) or 4x the chrominance sampling rate (6.75 MHz), all signals are reference to rising edge.
2. In accordance with CCIR656, the input pixel pattern begins during the first clk period after the falling edge of HSYNC (same for master mode and slave mode). The input pattern is Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3,..... The input pin CBSWAP and md[3] (YCSWAP) could be used to swap cb, cr sequence and also y and cb, cr sequence. See **Figure 3**.
3. Pixel input range: See **Table 4**

   Y: 16-235 for normal range; 0-15, 236-255 are invalid. When Y value is between 0-15 then clamp to 16, when 236 and 255 Y will be set to 255.

   CbCr: 16-240 for normal range with 128 mapped to 0; 0-15, 241-255 are invalid. When Cb/Cr is between 0-15 will be clamp to 16, when Cb/Cr is 241 to 255 then will be set to 240.

Table-4 75% amplitude, 100% saturated YCbCr color bars

element	range	White	Yellow	Cyan	Green	Magenta	Red	Blue	black
Y	16-235	235	162	131	112	84	65	35	16
Cb	16-240	128	44	156	72	184	100	212	128
Cr	16-240	128	142	44	58	198	212	114	128

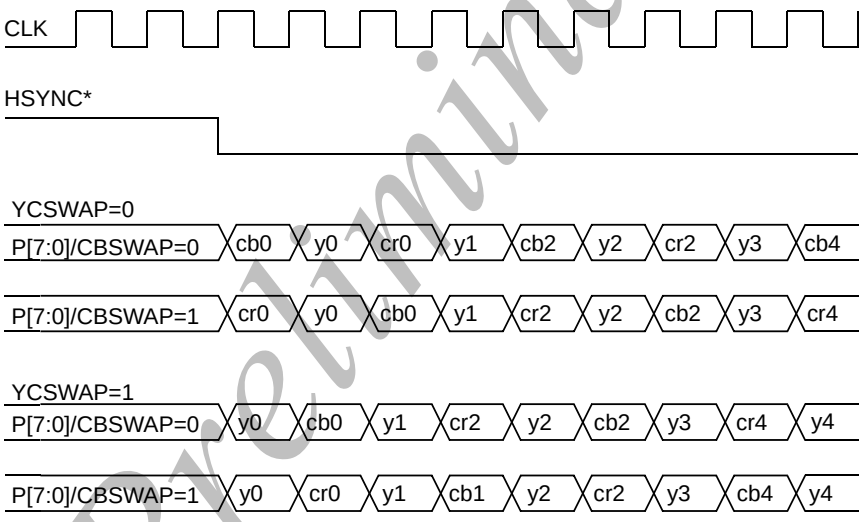


Figure-3

VIDEO TIMING

See **Table 5**, **Table 6**

1. If master mode is selected, horizontal counter is incremented on clk/2, and reset to 1 when h-total is hit. The output hsync is 6 clk later than the internal horizontal sync. Vertical counter is incremented by every horizontal scan line and reset to 1 after v-total hit. The output vertical sync is 3 or 2.5 lines for 262/525 and 312/625 later.
2. If slave mode is selected, the horizontal counter is incremented on the rising of clk and then reset to 1 after 2 clk cycles late of falling edge of hsync. The vertical counter is incremented on the falling edge of hsync and reset to 1 at falling edge of vertical sync. If the falling edge of vertical sync occurring within [-1/4,1/4] of a scan line from the falling edge of hsync indicates the even field, if within [-1/4,1/4] of middle point of scan line indicates odd field.
3. The width of horizontal sync and the start and end of color burst is automatically calculated and inserted for each mode.
4. sync timing and burst envelopes are internally controlled. Color burst frequency is derived from the clk. Any jitter on clk may induce a color burst frequency error.
5. timing tables:

Table-5 Vertical timing table

System	Odd-field Non-active	Odd-field Active	Even-field Non-active	Even-field Active	Total size	Active size
NTSC	Line 1-22 VBI=7-21	Line 23-262	Line 263-284; 525 VBI=270-284	Line 285-524	858*525	720*480
PAL-BD°K.	Line 1-22 VBI=7-21	Line 23-310	Line 311-335; 624, 625 VBI=319-333	Line 336-623	864*625	720*576

Table-6 Horizontal timing table: number of 13.5 MHz cycles

System	Front-porch	Back-porch	Active	Burst-start	Burst-width	total
NTSC	20	127(122)	711	72	34	858
PAL-M	20	127	711	78	34	858
PAL-BD..	20	142(132)	702	76	30	864
PAL-Nc	20	142	702	76	34	864

6. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. For NTSC, color burst information is automatically disabled on scan line 1-9 and 264-272 or PAL-M, color burst information is automatically disabled on scan line 1-11 and 263-273. For PAL-BDGHINc, color burst information is automatically disabled on scan line 1-6 and 310-318 and 623-625 for field 1,2,5,6. However, for field 3,4,7,8 burst is disabled at scan line 1-5,311-319,622-625. See the following **Figure 4**, **Figure 5** and **Figure 6**.

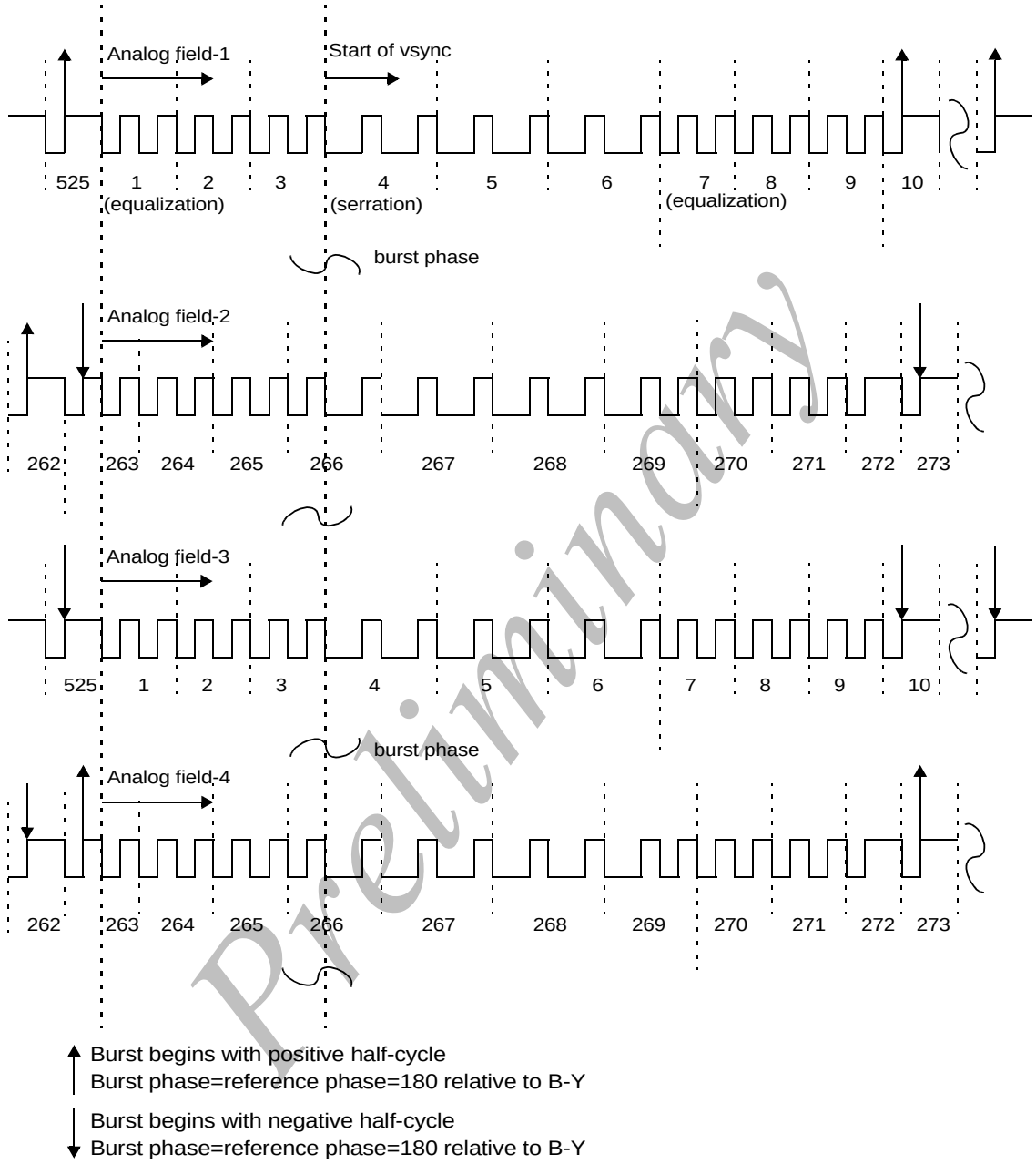


Figure-4 Interface 525-line (NTSC) video timing

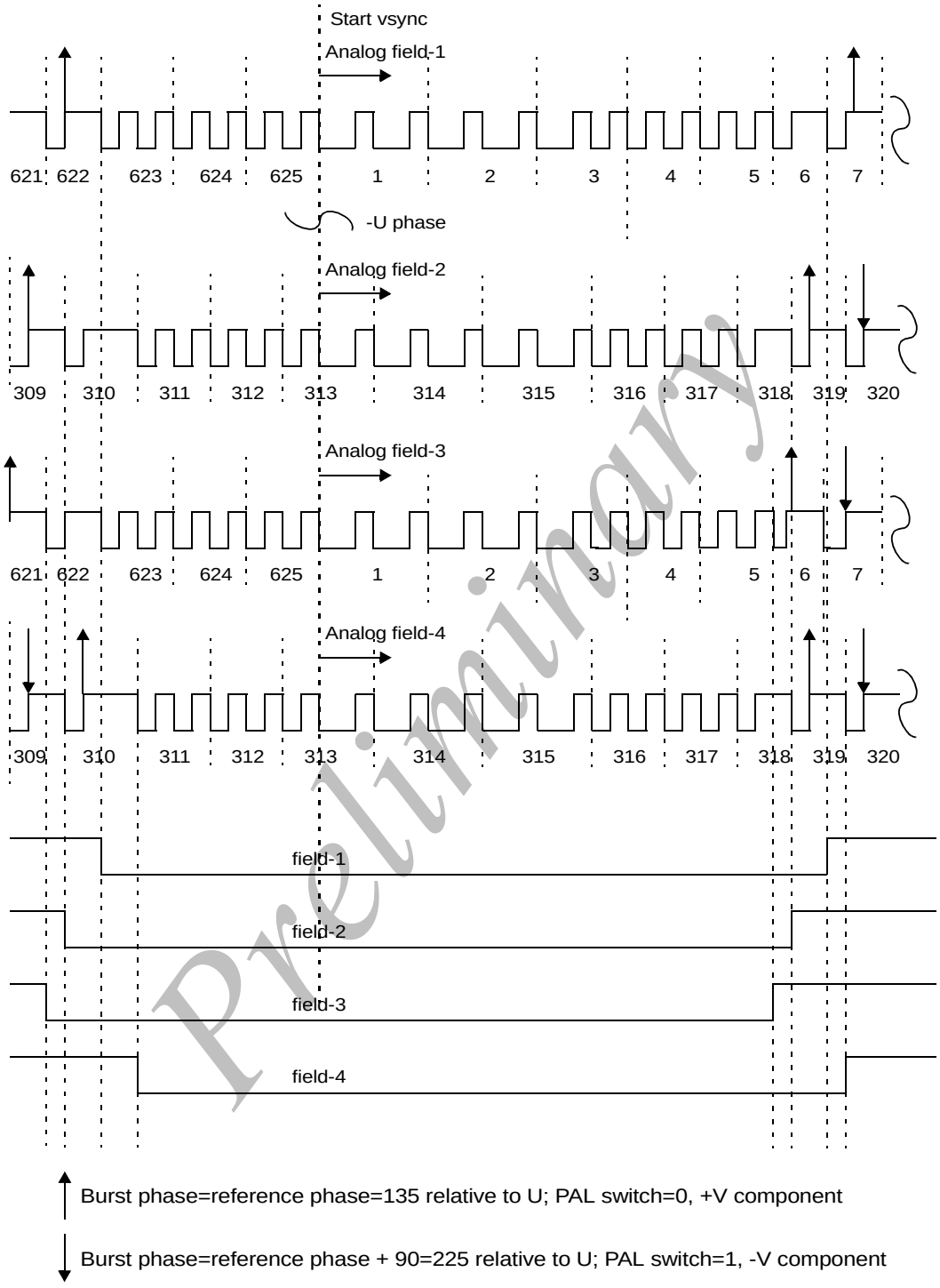


Figure-5 Interface 625-line (PAL-B,D,G,H,I,N,Nc) video timing

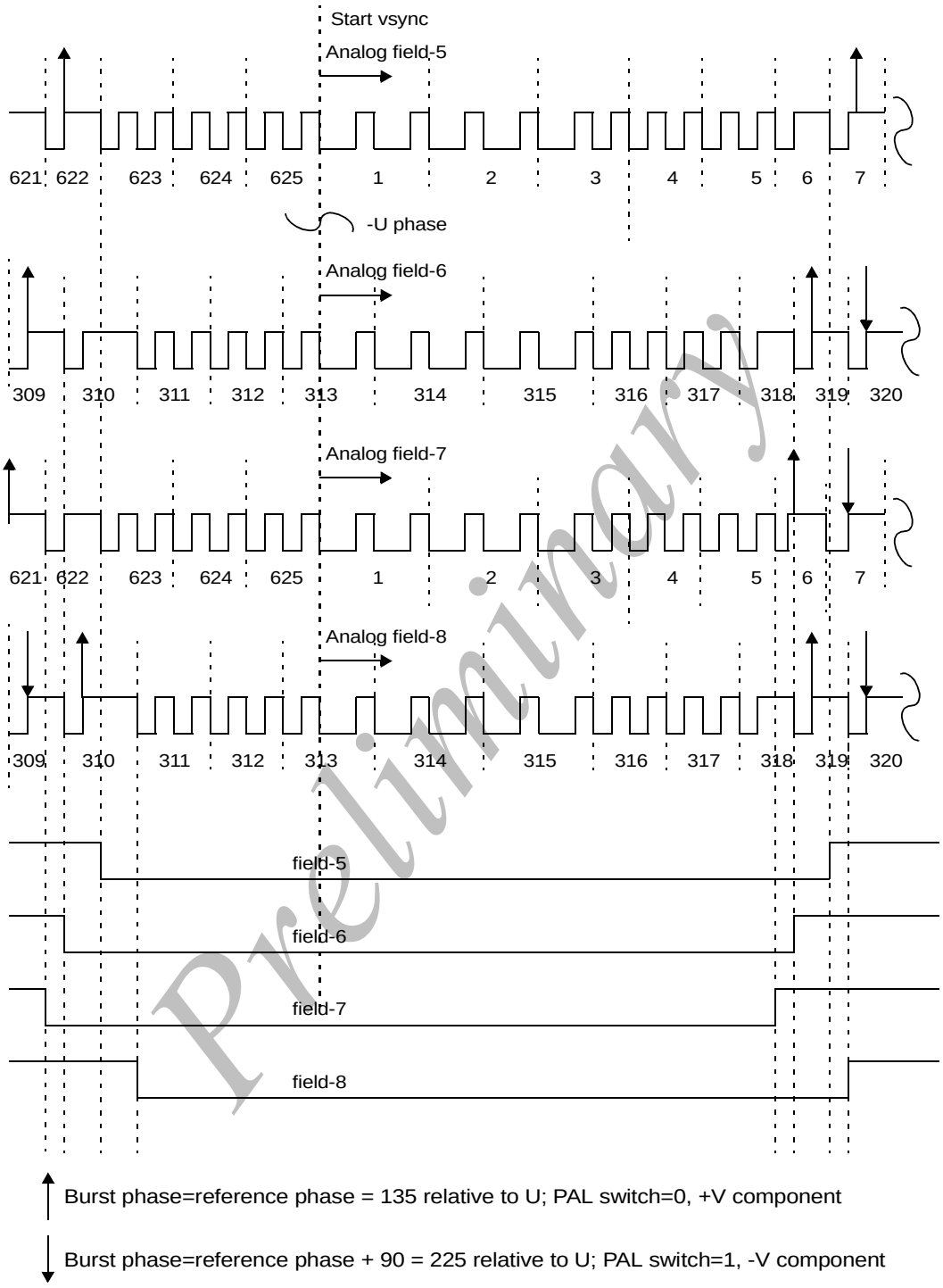


Figure-6

ANTI-ALIAS FILTERS CHARACTERIS

The Y and the U, V are up-samples to clk, 27MHz after 4:2:2 to 4:4:4 conversion. Y is filtered by a filter whose passband is 6MHz. And U, V are also filtered by passband = 1.3MHz filters.

Please refer to **Figure 7** to **Figure 10**

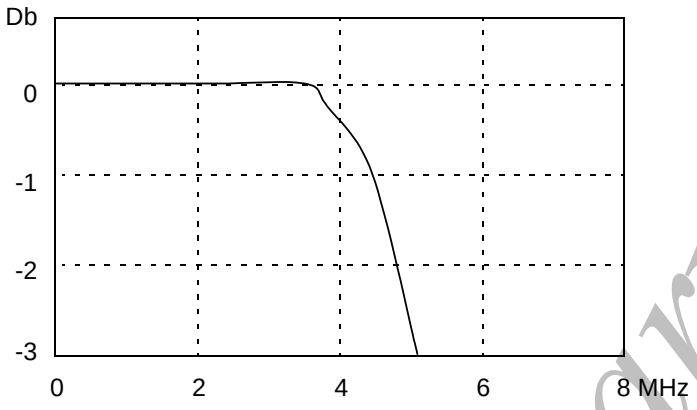


Figure-7 2X Sample Y filter frequency response/passband

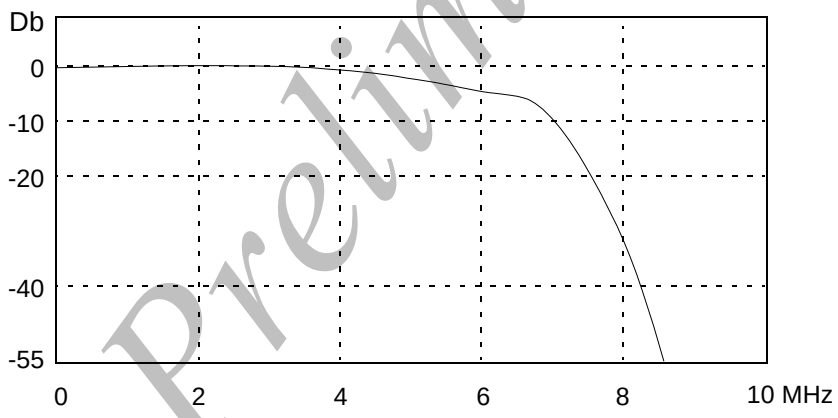


Figure-8 2X Sample Y filter frequency response/stopband

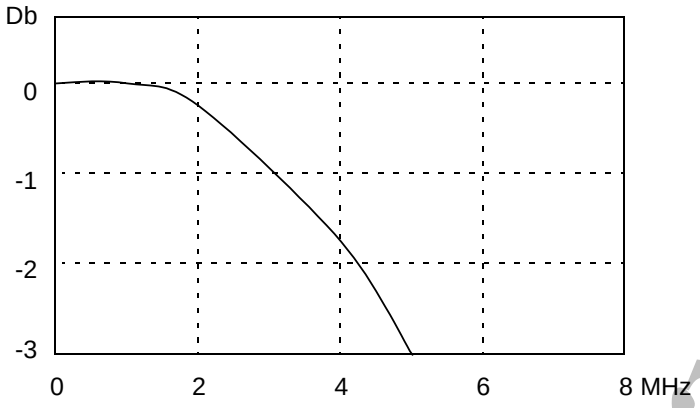


Figure-9 2X U/V filter frequency response/passband

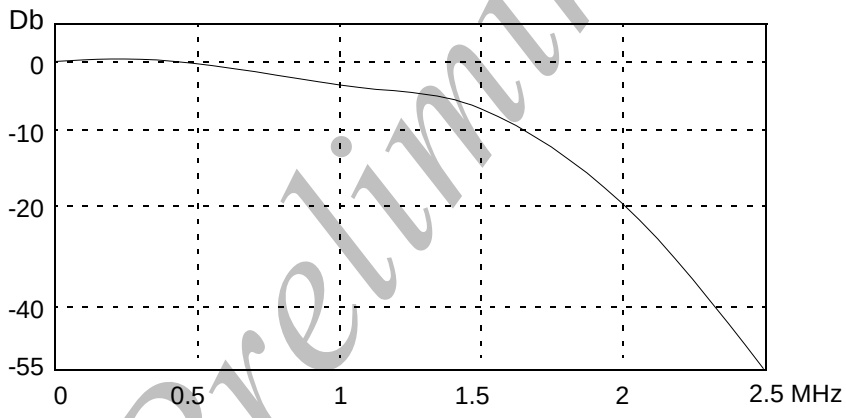


Figure-10 2X U/V filter frequency response/stopband

DAC MAPPING

Depends on the video output mode, the color bars mapping to DAC are specified in **Table 7** to **Table 12** and **Figure 11** to **Figure 16**. Where white is 400. For PAL-BDGHINc blank = 120. For NTSC/PAL-M blank = 114 (setup = 0), 1 IRE = 2.857; if setup = 1, blank = 112, 1 IRE = 2.8.

Table-7 s-video Y NTSC/PAL-M 525, setup = 0

Description	DAC data	Sync interval
White	400	0
Black	136	0
Blank	114	0
Sync	0	1

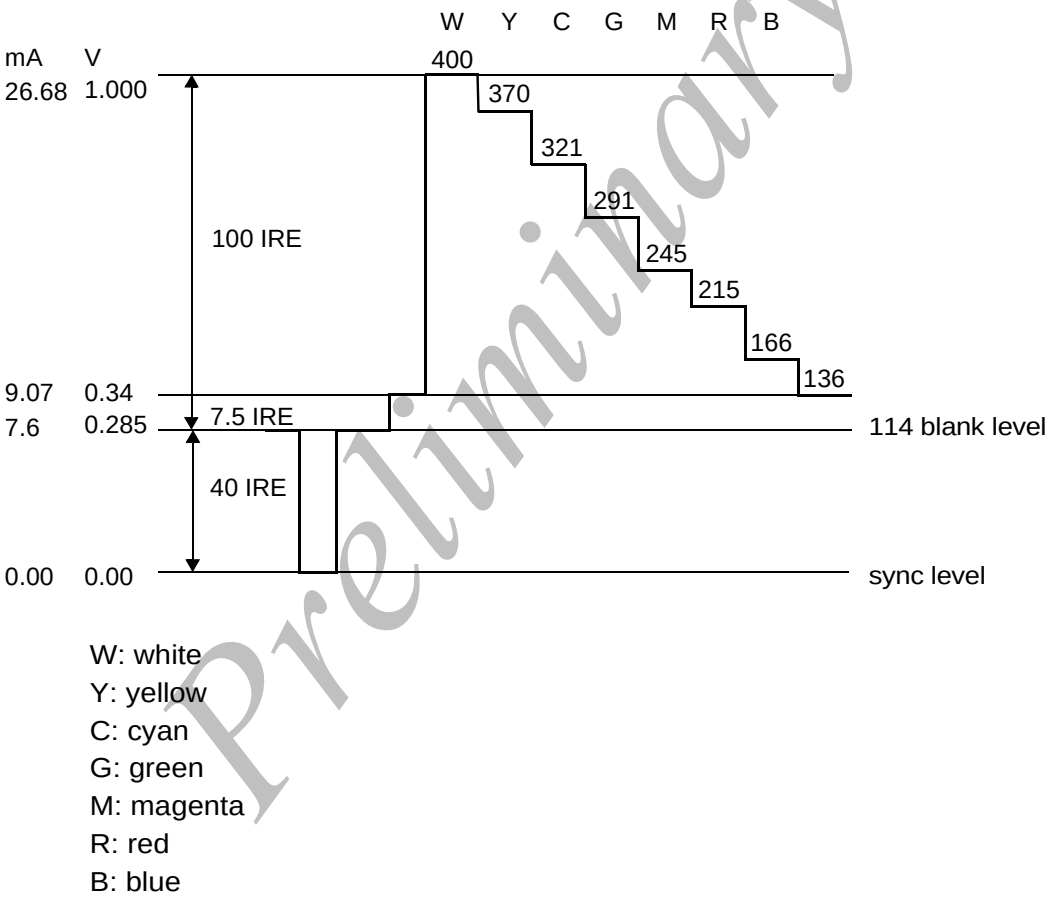


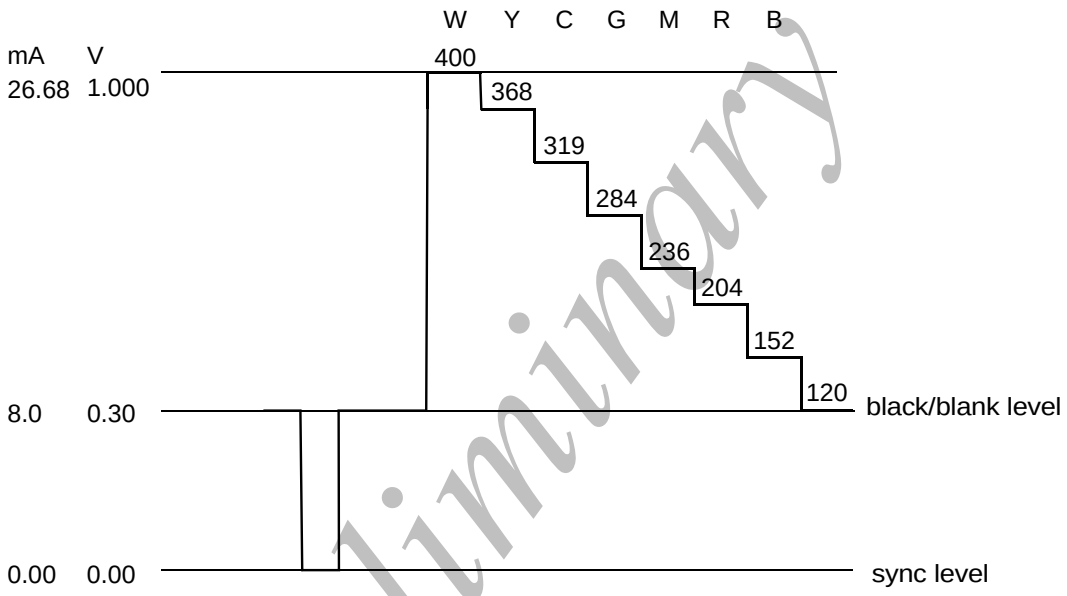
Figure-11 Color bars, s-video Y NTSC/PAL-M 525, setup=0 video output waveform

Table-8 s-video Y PAL-BDGHINc 625

Description	DAC data	Sync interval
White	400	0
Black	120	0
Blank	120	0
Sync	0	1

Typical with 37.5Ω load, vref_o = vref_i, SETUP = 0

100% saturation (100/0/100/0) color bars.



W: white
Y: yellow
C: cyan
G: green
M: magenta
R: red
B: blue

Figure-12 color bars, s-video Y PAL-BDGHINc 625 video output waveform

Table-9 s-video Chrominance NTSC/PAL-M 525

Typical with 37.5Ω load, vref_o = vref_i, SETUP = 0

100% saturation color bars.

Description	DAC data	Sync interval
Peak C (high)	423	No
Burst (high)	313	No
Blank	256	No
Burst (low)	199	No
Peak C (low)	89	No

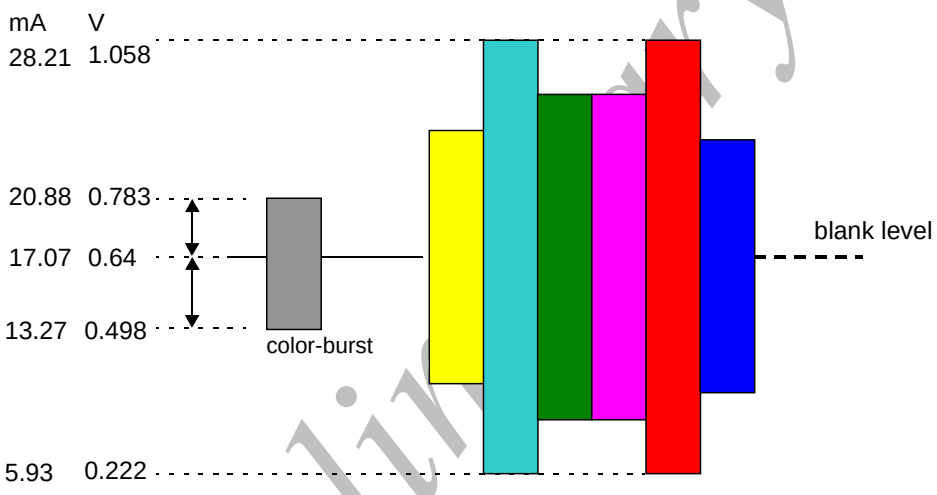


Figure-13 color bars, s-video Chrominance NTSC/PAL-M 525 video output waveform

Table-10 s-video Chrominance PAL-BDGNICc 625

Typical with 37.5Ω load, vref_o = vref_i, SETUP = 0

100% saturation (100/0/100/0) color bars.

Description	DAC data	Sync interval
Peak C (high)	433	No
Burst (high)	316	No
Blank	256	No
Burst (low)	196	No
Peak C (low)	79	No

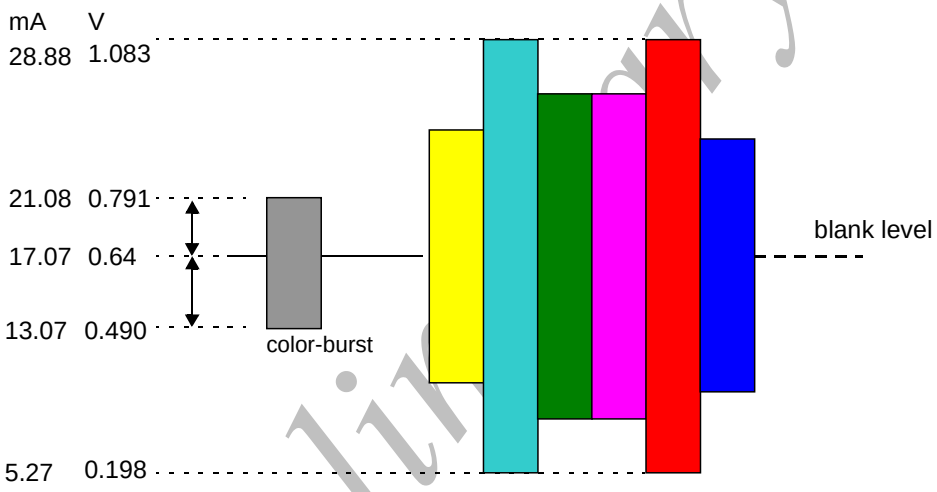


Figure-14 color bars, s-video Chrominance PAL-BDGNICc video output waveform

Table-11 composite NTSC/PAL 525

Typical with 37.5Ω load, vref_o = vref_i, SETUP = 0

100% saturation color bars.

Description	DAC data	Sync interval
Peak C (high)	488	0
White	400	0
Burst (high)	171	0
Black	136	0
Blank	114	0
Burst (low)	57	0
Peak C (low)	48	0
Sync	0	1

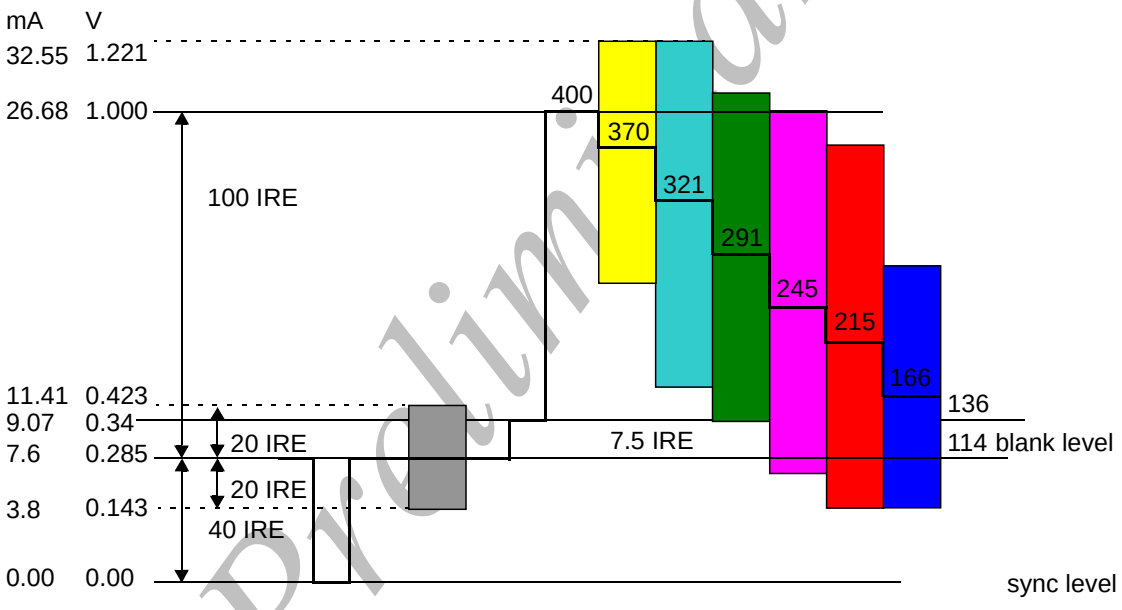


Figure-15 colors, composite NTSC/PAL 525 video output waveform

Table-12 composite PAL-BDGHINc 625

Typical with 37.5Ω load, vref_o = vref_i, SETUP = 0

100% saturation (100/0/100/0) color bars.

Description	DAC data	Sync interval
Peak C (high)	488	0
White	400	0
Burst (high)	171	0
Black	136	0
Blank	114	0
Burst (low)	57	0
Peak C (low)	48	0
Sync	0	1

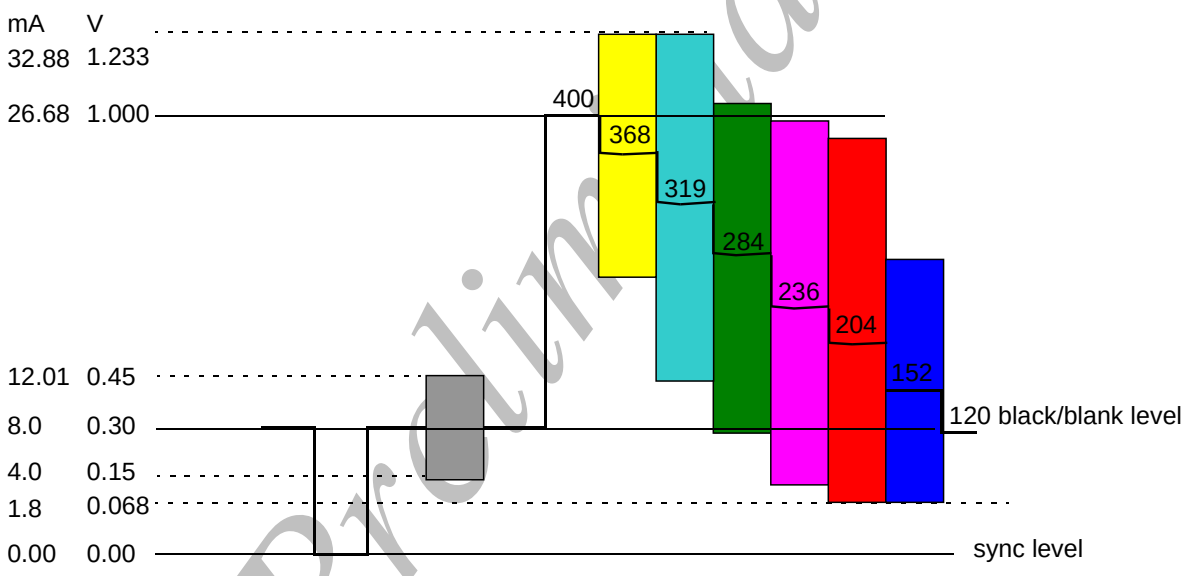


Figure-16 Colors, composite PAL-BDGHINc 625 video output waveform

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VAA	Power Supply	3.0	3.3	3.6	V
TA	Ambient Operating Temperature	0	-	70	°C
RL	DAC Output Load		37.5	--	Ω
VREF_IN	External Voltage Reference	1.11	1.23	1.35	V
	Nominal REST		850		Ω

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
VAA	Power Supply (Measured to ground)	--	--	5	V
TA	Ambient Operating Temperature	-55	--	125	°C
	Voltage on Any Signal Pin	GND-0.3		VAA+0.3	V
TS	Storage Temperature	-65		+150	°C
TJ	Junction Temperature			+150	°C

DC CHARACTERISTICS

(Recommended operating conditions using external voltage reference with RSET = 850Ω, VREFIN = 1.23V, NTSC CCIR601 operation and clock frequency = 27MHz at 25°C, +3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
IAA	VAA Supply Current			105	mA
	Video D/A Resolution	9	9	9	Bits
INL	Integral Nonlinearity			± 1	LSB
DNL	Differential Nonlinearity			± 1	LSB
	Maximum Output Current			35	mA
VOC	Output Compliance	0		1.5	V
	Video level Error			5	%
	Full-Scale DAC Output		182.5		IRE
	Digital Inputs				
VIH	Input High Voltage	2.0		VAA+0.3	V
VIL	Input Low Voltage	GND-0.3		0.8	V
IIH	Input High current (Vin=2.4V)			1	µA
IIL	Input Low current (Vin=0.4V)			-1	µA
	Digital Outputs				
VOH	Output High Voltage (IOH=-400µA)	2.4			V
VOL	Output Low Voltage (IOL=3.2mA)			0.4	V
IOZ	Three-State Current			50	µA
VREF_IN	VREF_IN Input Current		10		µA
VREF_OUT	VREF_OUT Output Voltage	1.11	1.23	1.35	V
IREF_OUT	VREF_OUT current		10		µA

AC CHARACTERISTICS

(Recommended operating conditions using external voltage reference with RSET = 850Ω, VREFIN = 1.23V, NTSC CCIR601 operation and clock frequency = 27MHz at 25°C, +3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
	Luminance Bandwidth		$F_{ck}/4$		MHz
	Chrominance Bandwidth		1.3		MHz
	Differential Gain		1		%
	Differential Phase		1		°
	SNR		60		dB
	Hue Accuracy		1.5	3	°
	Color Saturation Accuracy		1.5	3	%
4	Analog Output Delay		30		ns
	Analog Output Rise Time		3		ns
	Analog Output Setting Time		30		ns
1	Pixel/Control Setup Time	1			ns
2	Pixel/Control Hold Time	3			ns
3	Control Output Delay Time		15		ns
F_{ck}	CLOCK Frequency	24.54	27	29.5	MHz
	CLOCK Pulse Width Low Time	10			ns
	CLOCK Pulse Width High Time	10			ns

Video Input and Output Timing

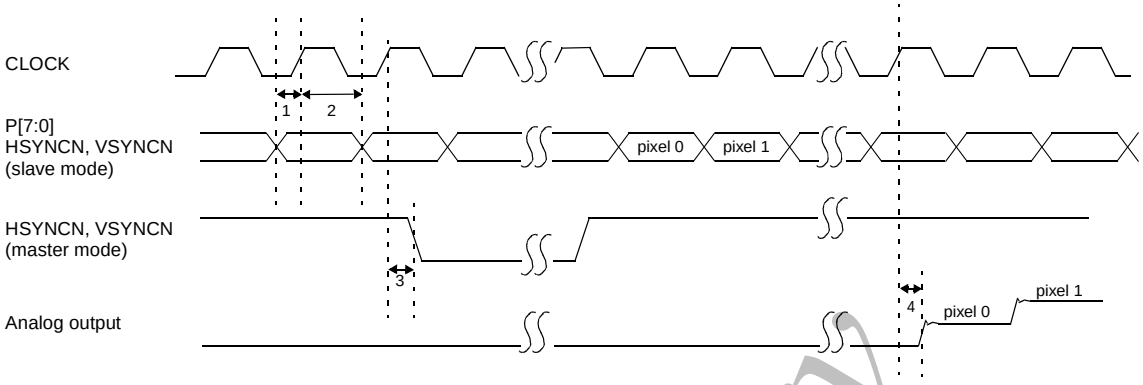
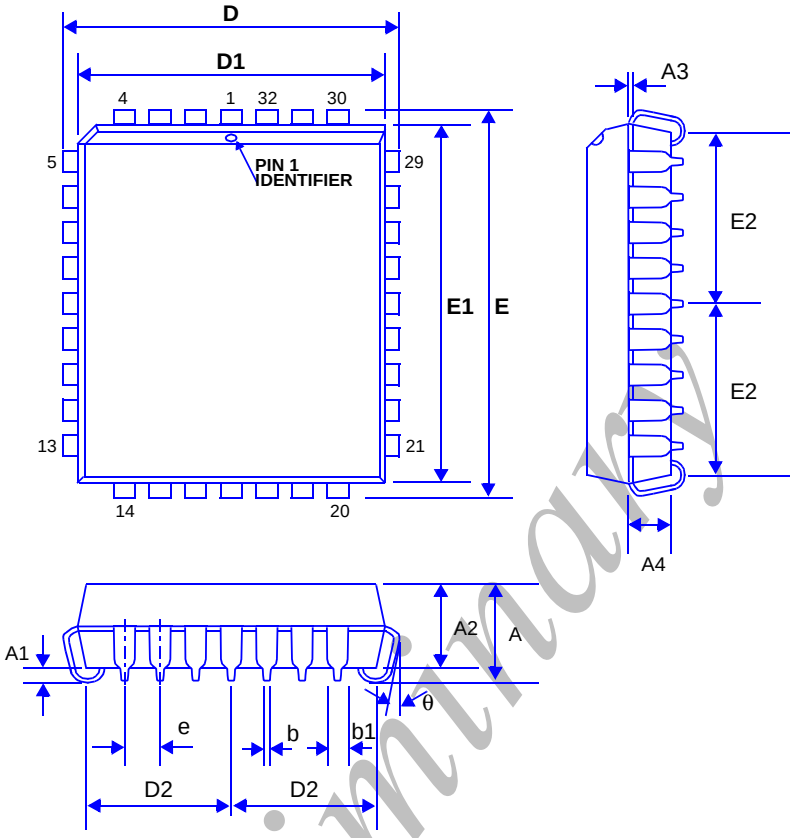


Figure-17 Video Input and Output Timing

PACKAGE OUTLINE (32-pin PLCC)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	3.56	-	-	0.14
A1	0.50	-	-	0.020	-	-
A2	2.79 REF			0.110 REF		
A3	0.20	-	0.35	0.008	-	0.014
A4	1.91	2.29	2.41	0.075	0.090	0.095
b	0.40	-	0.53	0.016	-	0.021
b1	0.66	-	0.81	0.026	-	0.032
D	12.32	12.45	12.57	0.485	0.490	0.495
D1	11.35	11.43	11.51	0.447	0.450	0.453
D2	5.21 REF			0.205 REF		
E	14.86	14.99	15.11	0.585	0.590	0.595
E1	13.89	13.97	14.05	0.547	0.550	0.553
E2	6.48 REF			0.255 REF		
e	1.27 REF			0.050 REF		
θ	0°	–	10°	0°	–	10°