3A, 12V, Synchronous-Rectified Buck Converter

Features

- Wide Input Voltage from 4.3V to 14V
- Output Current up to 3A
- Adjustable Output Voltage from 0.8V to V_{IN}
  - ±2% System Accuracy
- 70mW Integrated Power MOSFETs
- High Efficiency up to 95%
  - Automatic Skip/PWM Mode Operation
- Current-Mode Operation
  - Easy Feedback Compensation
  - Stable with Low ESR Output Capacitors
  - Fast Load/Line Transient Response
- Power-On-Reset Monitoring
- Fixed 500kHz Switching Frequency in PWM mode
- Built-in Digital Soft-Start and Soft-Stop
- Current-limit Protection with Frequency Foldback
- 118% Overvoltage Protection
- Hiccup-mode 50% Undervoltage Protection
- Over-Temperature Protection
- <3mA Quiescent Current in Shutdown Mode
- Small SOP-8 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- OLPC, UMPC
- Notebook Computer
- Handheld Portable Device
- Step-down Converters Requiring High Efficiency and 3A Output Current

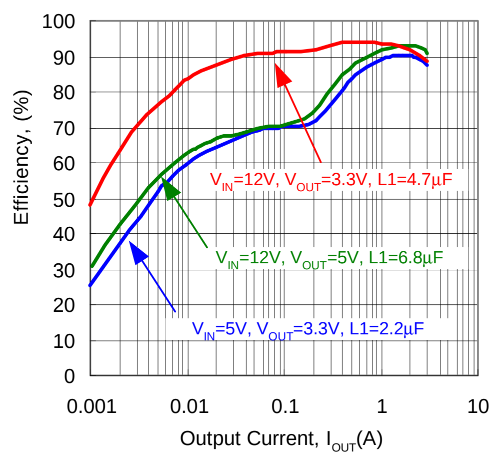
General Description

The APW7142 is a 3A synchronous-rectified Buck converter with integrated 70mΩ power MOSFETs. The APW7142, designed with a current-mode control scheme, can convert wide input voltage of 4.3V to 14V to the output voltage adjustable from 0.8V to VIN to provide excellent output voltage regulation.

For high efficiency over all load current range, the APW7142 is equipped with an automatic Skip/PWM mode operation. At light load, the IC operates in the Skip mode, which keeps a constant minimum inductor peak current, to reduce switching losses. At heavy load, the IC works in PWM mode, which inductor peak current is programmed by the COMP voltage, to provide high efficiency and excellent output voltage regulation .

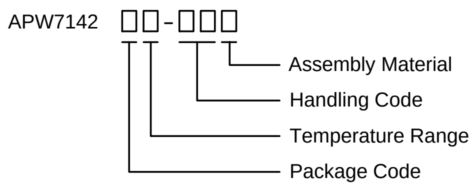
The APW7142 is also equipped with power-on-reset, soft-start, soft-stop and whole protections (undervoltage, overvoltage, over temperature and current-limit) into a single package. In shutdown mode, the supply current drops below 3µA.

This device, available in an 8-pin SOP-8 package, provides a very compact system solution with minimal external components and PCB area.



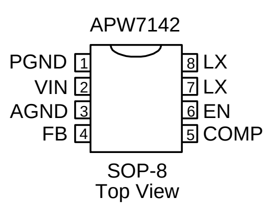
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

	Package Code K : SOP-8 Operating Junction Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7142 K : [APW7142 XXXXX]	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 2)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to AGND)		-0.3 ~ 15	V
V_{LX}	LX to GND Voltage	> 100ns	-1 ~ V_{IN}+1	V
		< 100ns	- 5 ~ V_{IN}+5	
	PGND to AGND Voltage		-0.3 ~ +0.3	V
	EN to AGND Voltage		-0.3 ~ V_{IN}+0.3	V
	FB, COMP to AGND Voltage		-0.3 ~ 6	V
P_D	Power Dissipation		Internally Limited	W
	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note 2 : Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 3) SOP-8	80	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.3 ~ 14	V
V_{OUT}	Converter Output Voltage	0.8 ~ V_{IN}	V
I_{OUT}	Converter Output Current	0 ~ 3	A
C_{IN}	Converter Input Capacitor (MLCC)	8 ~ 50	μF
C_{OUT}	Converter Output Capacitor	20 ~ 1000	μF
	Effective Series Resistance	0 ~ 60	mΩ
L_{OUT}	Converter Output Inductor	1 ~ 22	μH
	Resistance of the Feedback Resistor connected from FB to GND	1 ~ 20	kΩ
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the Typical Application Circuits

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7142			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB} = V_{REF} +50mV, V_{EN}=3V, LX=NC	-	0.5	1.5	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN} = 0V	-	-	3	μA
POWER-ON-RESET (POR) VOLTAGE THRESHOLD						
	VIN POR Voltage Threshold	V_{IN} rising	3.9	4.1	4.3	V
	VIN POR Hysteresis		-	0.5	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Regulated on FB pin	-	0.8	-	V
	Output Voltage Accuracy	T_J = 25°C, I_{OUT}=10mA, V_{IN}=12V	-1.0	-	+1.0	%
		I_{OUT}=10mA~3A, V_{IN}=4.75~14V	-2.0	-	+2.0	%
	Line Regulation	V_{IN} = 4.75V to 14V	-	+0.02	-	%/V
	Load Regulation	I_{OUT} = 0.5A ~ 3A	-	-0.04	-	%/A
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency	T_J = -40 ~ 125°C, V_{IN} = 4.75 ~ 14V	450	500	550	kHz
	Foldback Frequency	V_{OUT} = 0V	-	80	-	kHz
	Maximum Converter's Duty		-	99	-	%
T_{ON_MIN}	Minimum Pulse Width of LX		-	150	-	ns
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance	V_{FB}=V_{REF}±50mV	-	200	-	μA/V
	Error Amplifier DC Gain	COMP = NC	-	80	-	dB

Electrical Characteristics (Cont.)

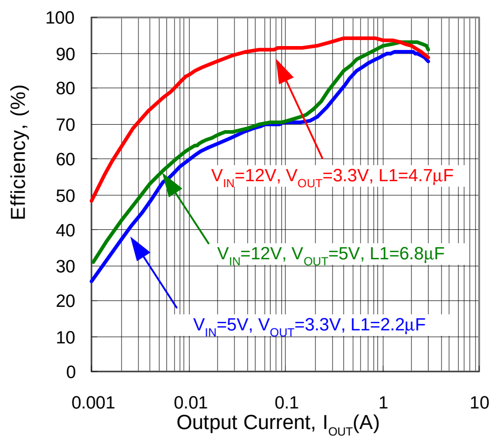
Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7142			Unit
			Min	Typ	Max	
	Current-Sense to COMP Voltage Transresistance		-	0.048	-	V/A
	High-side Switch Resistance	V_{IN} = 5V, T_J=25°C	-	90	110	mΩ
		V_{IN} = 12V, T_J=25°C	-	70	90	
	Low-side Switch Resistance	V_{IN} = 5V, T_J=25°C	-	90	110	mΩ
		V_{IN} = 12V, T_J=25°C	-	70	90	
PROTECTIONS						
I_{LIM}	High-side Switch Current-limit	Peak Current	4.0	5.5	7.0	A
V_{TH_UV}	FB Under-voltage Threshold	V_{FB} falling	45	50	55	%
V_{TH_OV}	FB Over-voltage Threshold	V_{FB} rising	114	118	122	%
	FB Under-Voltage Debounce		-	1	-	μs
T_{OTP}	Over-temperature Trip Point		-	150	-	°C
	Over-temperature Hysteresis		-	40	-	°C
T_D	Dead-Time	V_{LX} = -0.7V	-	20	-	ns
SOFT-START, SOFTSTOP, ENABLE AND INPUT CURRENTS						
T_{SS}	Soft-Start / Soft-Stop Interval		1.5	2	2.5	ms
	EN Shutdown Voltage Threshold	V_{EN} falling	0.5	-	-	V
	EN Enable Voltage Threshold		-	-	2.1	V
	High-side Switch Leakage Current	V_{EN} = 0V, V_{LX} = 0V	-	-	2	μA
I_{FB}	FB Pin Input Current		-100	-	+100	nA
I_{EN}	EN Pin Input Current	V_{EN} = 0V ~ V_{IN}	-100	-	+100	nA

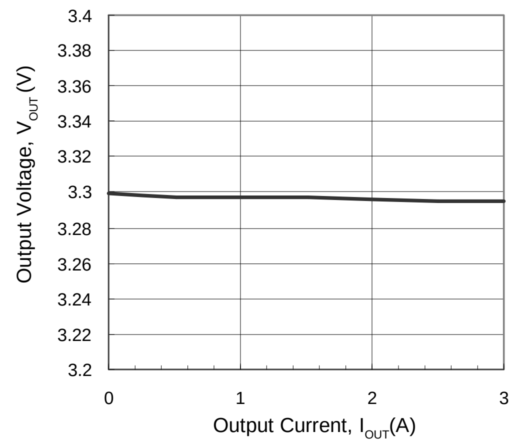
Typical Operating Characteristics

(Refer to the application circuit 1 in the section “Typical Application Circuits”, V_{IN}=12V, V_{OUT}=3.3V, L1=4.7µH)

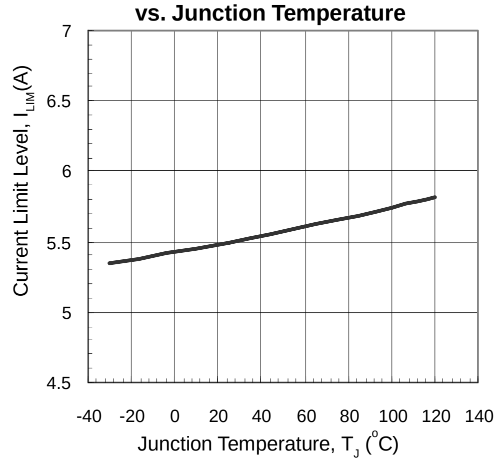
Output Current vs. Efficiency



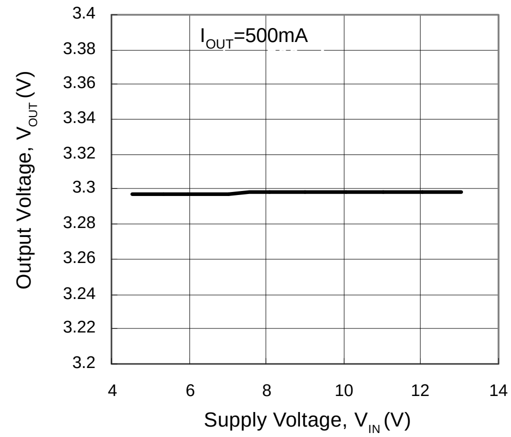
Output Voltage vs. Output Current



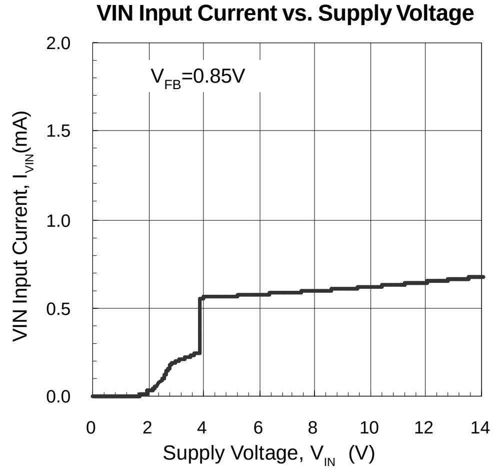
Current Limit Level (Peak Current) vs. Junction Temperature



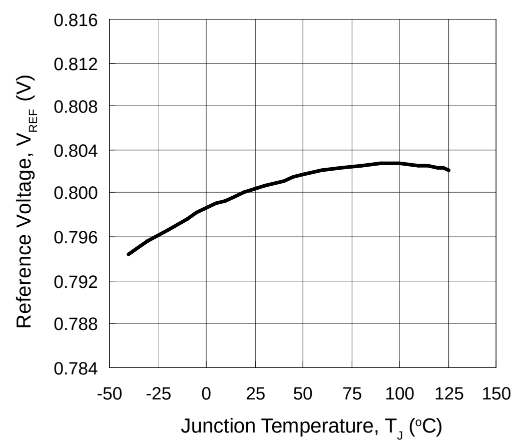
Output Voltage vs. Supply Voltage



VIN Input Current vs. Supply Voltage



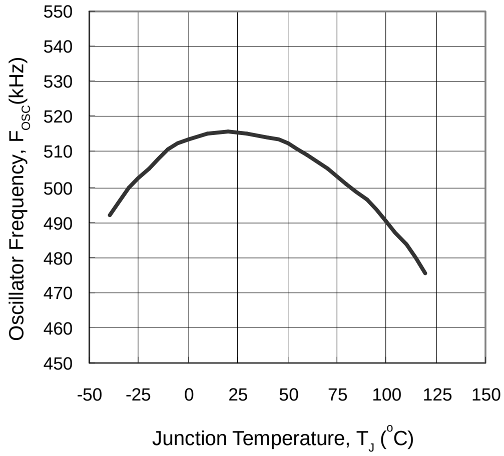
Reference Voltage vs. Junction Temperature



Typical Operating Characteristics (Cont.)

(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=4.7μH)

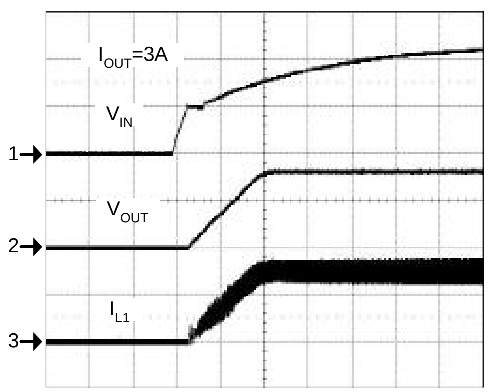
Oscillator Frequency vs. Junction Temperature



Operating Waveforms

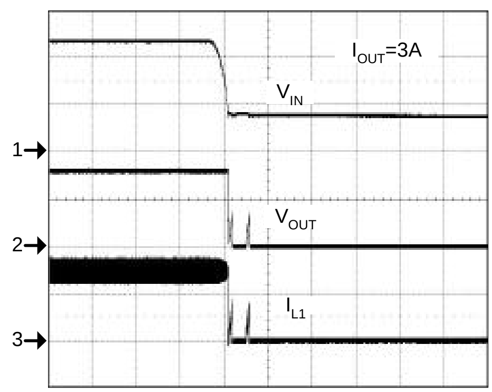
(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=4.7μH)

Power On



CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{L1} , 2A/div
Time : 1ms/div

Power Off

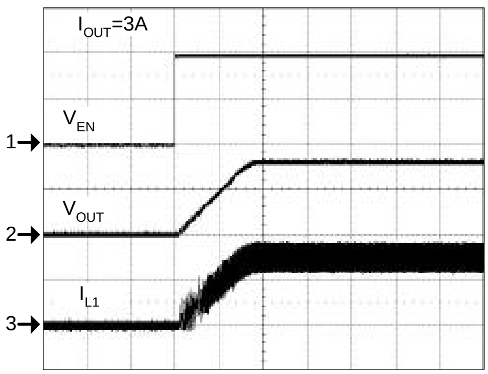


CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{L1} , 2A/div
Time : 10ms/div

Operating Waveforms (Cont.)

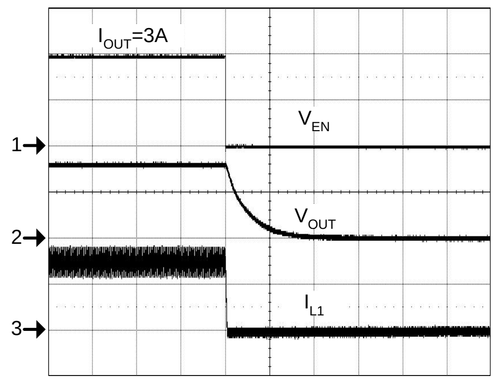
(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=4.7μH)

Enable



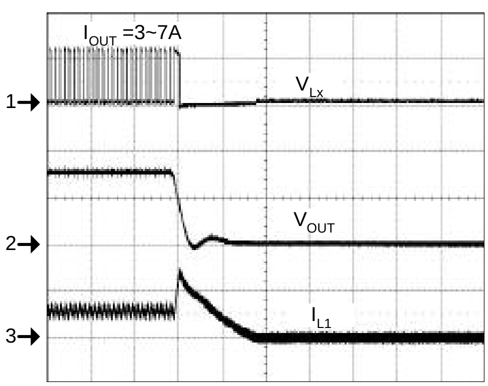
CH1 : V_{EN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{L1} , 2A/div
Time : 1ms/div

Shutdown



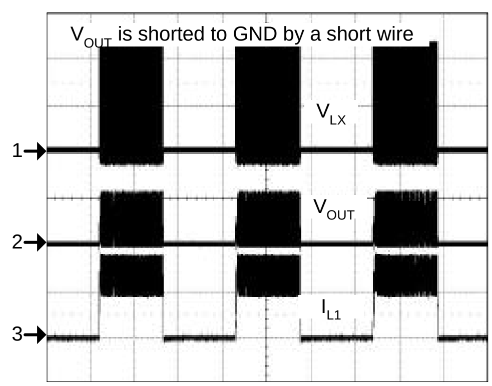
CH1 : V_{EN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{L1}, 2A/div
Time : 100μs/div

Short Circuit



CH1 : V_{LX} , 10V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{L1} , 5A/div
Time : 20μs/div

Short Circuit

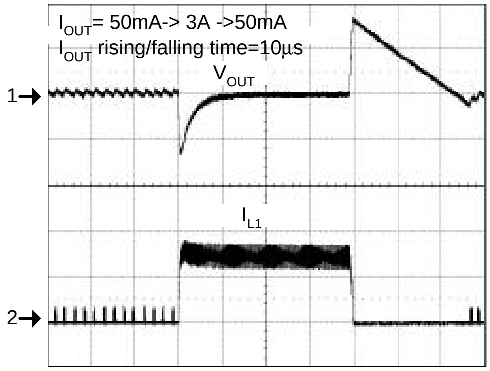


CH1 : V_{LX} , 5V/div
CH2 : V_{OUT} , 200mV/div
CH3 : I_{L1} , 5A/div
Time : 5ms/div

Operating Waveforms (Cont.)

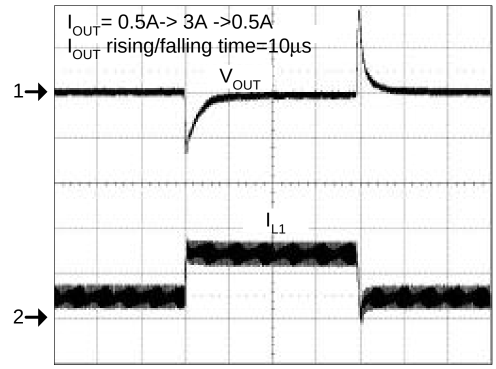
(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=4.7µH)

Load Transient Response



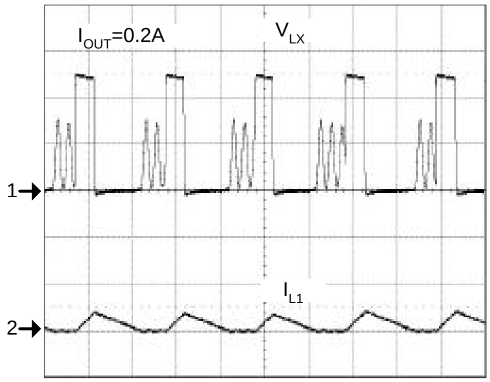
CH1 : V_{OUT} , 200mV/div
CH2 : I_{L1} , 2A/div
Time : 100µs/div

Load Transient Response



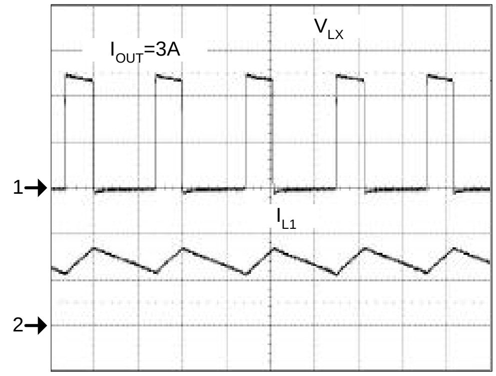
CH1 : V_{OUT} , 100mV/div
CH2 : I_{L1} , 2A/div
Time : 100µs/div

Switching Waveform



CH1 : V_{LX} , 5V/div
CH2 : I_{L1} , 2A/div
Time : 1µs/div

Switching Waveform

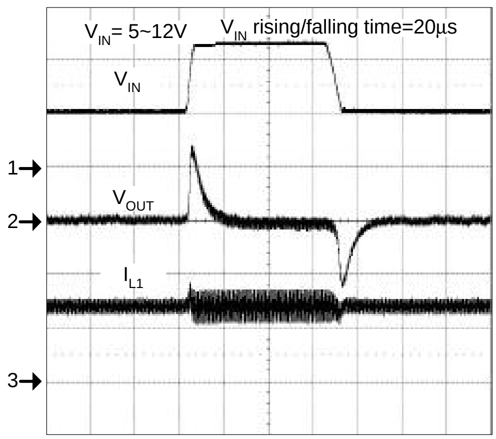


CH1 : V_{LX} , 5V/div
CH2 : I_{L1} , 2A/div
Time : 1µs/div

Operating Waveforms (Cont.)

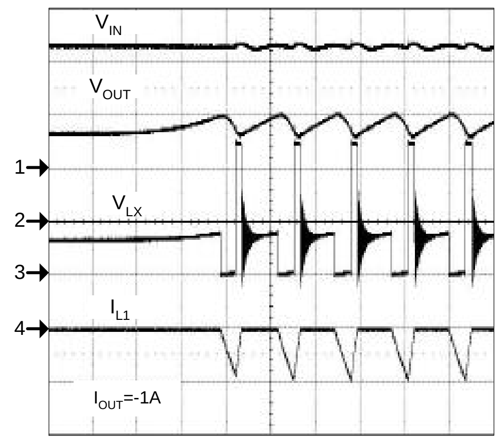
(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=4.7μH)

Line Transient



CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 50mV/div (Voffset=3.3V)
CH3 : I_{L1} , 2A/div
Time : 100μs/div

Over Voltage Protection

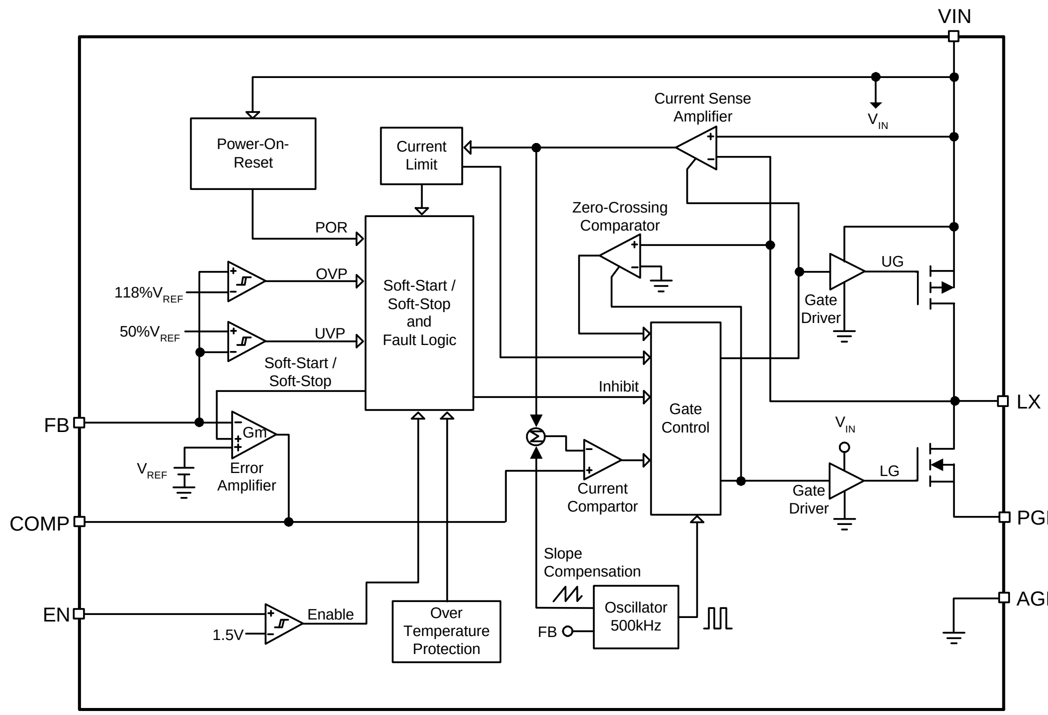


CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : V_{LX} , 5V/div
CH4 : I_{L1} , 5A/div
Time : 20μs/div

Pin Description

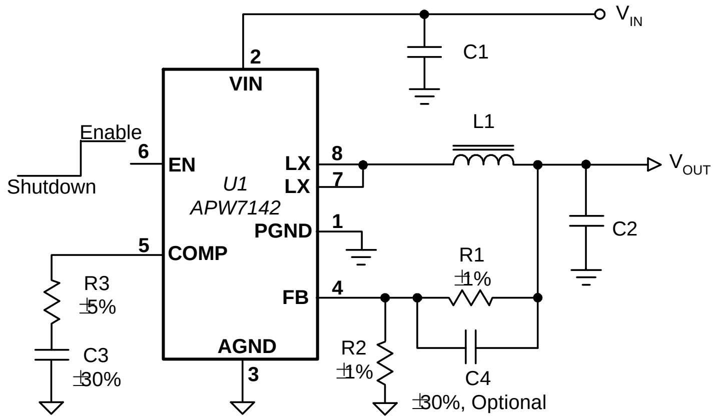
PIN No.	NAME	FUNCTION
1	PGND	Power Ground of the APW7142, which is the source of the N-channel power MOSFET. Connect this pin to system ground with lowest impedance.
2	VIN	Power Input. VIN supplies the power (4.3V to 14V) to the control circuitry, gate drivers and step-down converter switches. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and both of AGND and PGND eliminates switching noise and voltage ripple on the input to the IC.
3	AGND	Ground of MOSFET Gate Drivers and Control Circuitry.
4	FB	Output feedback Input. The APW7142 senses the feedback voltage via FB and regulates the voltage at 0.8V. Connecting FB with a resistor-divider from the converter's output sets the output voltage from 0.8V to VIN.
5	COMP	Output of the error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
6	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect this pin to VIN if it is not used.
7, 8	LX	Power Switching Output. LX is the junction of the high-side and low-side power MOSFETs to supply power to the output LC filter.

Block Diagram



Typical Application Circuits

1. 4.3~14V Single Power Input Step-down Converter (with a Ceramic Output Capacitor)



a. Cost-effective Feedback Compensation (C4 is not connected)

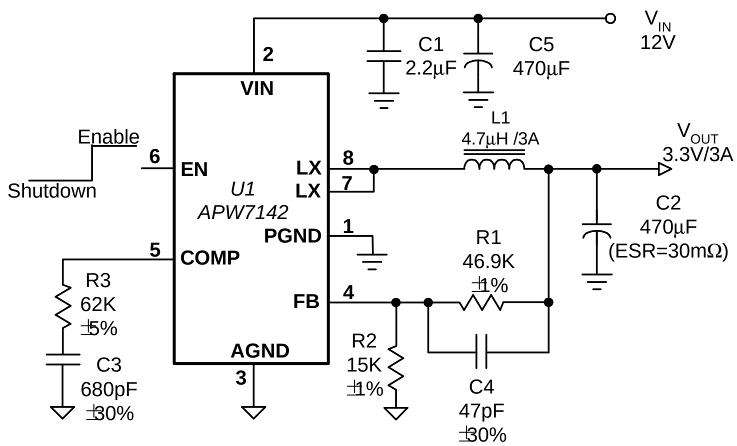
V_{IN}(V)	V_{OUT}(V)	L1(mH)	C2(mF)	C2 ESR(mW)	R1(kW)	R2(kW)	R3(kW)	C3(pF)
12	5	6.8	22	5	63.0	12	10.0	1500
12	5	6.8	44	3	63.0	12	20.0	1500
12	3.3	4.7	22	5	46.9	15	10.0	1500
12	3.3	4.7	44	3	46.9	15	22.0	1500
12	2	3.3	22	5	30.0	20	10.0	1500
12	2	3.3	44	3	30.0	20	20.0	1500
12	1.2	2.2	22	5	7.5	15	8.2	1800
12	1.2	2.2	44	3	7.5	15	16.0	1800
5	3.3	2.2	22	5	46.9	15	8.2	680
5	3.3	2.2	44	3	46.9	15	20.0	680
5	1.2	2.2	22	5	7.5	15	3.0	1800
5	1.2	2.2	44	3	7.5	15	7.5	1800

b. Fast-Transient-Response Feedback Compensation (C4 is connected)

V_{IN}(V)	V_{OUT}(V)	L1(mH)	C2(mF)	C2 ESR(mW)	R1(kW)	R2(kW)	C4(pF)	R3(kW)	C3(pF)
12	5	6.8	22	5	63.0	12	47	33.0	470
12	5	6.8	44	3	63.0	12	47	68.0	470
12	3.3	4.7	22	5	46.9	15	47	22.0	680
12	3.3	4.7	44	3	46.9	15	47	47.0	680
12	2	3.3	22	5	30.0	20	47	13.0	1200
12	2	3.3	44	3	30.0	20	47	27.0	1200
12	1.2	2.2	22	5	7.5	15	150	7.5	2200
12	1.2	2.2	44	3	7.5	15	150	15.0	2200
5	3.3	2.2	22	5	46.9	15	56	20.0	220
5	3.3	2.2	44	3	46.9	15	56	43.0	220
5	1.2	2.2	22	5	7.5	15	330	3.3	1800
5	1.2	2.2	44	3	7.5	15	330	8.2	1500

Typical Application Circuits (Cont.)

2. +12V Single Power Input Step-down Converter (with an Electrolytic Output Capacitor)



Function Description

VIN Power-On-Reset (POR)

The APW7142 keeps monitoring the voltage on VIN pin to prevent wrong logic operations which may occur when VIN voltage is not high enough for the internal control circuitry to operate. The VIN POR has a rising threshold of 4.1V (typical) with 0.5V of hysteresis.

During startup, the VIN voltage must exceed the enable voltage threshold. Then the IC starts a start-up process and ramps up the output voltage to the voltage target.

Digital Soft-Start

The APW7142 has a built-in digital soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp (V_{RAMP}), connected to one of the positive inputs of the error amplifier, rises up from 0V to 0.95V to replace the reference voltage (0.8V) until the voltage ramp reaches the reference voltage.

During soft-start without output overvoltage, the APW7142 converter's sinking capability is disabled until the output voltage reaches the voltage target.

Digital Soft-Stop

At the moment of shutdown controlled by EN signal, undervoltage event or over-temperature protection, the APW7142 initiates a digital soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage.

During soft-stop, the internal voltage ramp (V_{RAMP}) falls down rises from 0.95V to 0V to replace the reference voltage. Therefore, the output voltage falls down slowly at light load. After the soft-stop interval elapses, the soft-stop process ends and the the IC turns on the low-side power MOSFET.

Output Undervoltage Protection (UVP)

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The undervoltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the undervoltage threshold, the IC shuts down converter's output.

The undervoltage threshold is 50% of the nominal output voltage. The undervoltage comparator has a built-in 2µs noise filter to prevent the chips from wrong UVP shut-down caused by noise. The undervoltage protection works in a hiccup mode without latched shutdown. The IC will initiate a new soft-start process at the end of the preceding delay.

Function Description (Cont.)

Overvoltage Protection (OVP)

The overvoltage function monitors the output voltage by FB pin. Should the FB voltage increase over 118% of the reference voltage due to the high-side MOSFET failure, or for other reasons, the overvoltage protection comparator will force the low-side MOSFET gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the internal bonding wires. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver - a common problem for OVP schemes with a latch.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7142. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 40°C. The OTP designed with a 40°C hysteresis lowers the average T_J during continuous thermal overload conditions, increasing lifetime of the APW7142.

Enable/Shutdown

Driving EN to ground initiates a soft-stop process and then places the APW7142 in shutdown. When in shutdown, after the soft-stop process is completed, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to less than 3μA.

Current-Limit Protection

The APW7142 monitors the output current, flowing through the high-side power MOSFET, and limits the current peak at current-limit level to prevent loads and the IC from damages during overload or short-circuit conditions.

Frequency Foldback

The foldback frequency is controlled by the FB voltage. When the output is shorted to ground, the frequency of the oscillator will be reduced to about 80kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage on FB again approaches 0.8V.

Application Information

Setting Output Voltage

The regulated output voltage is determined by:

$$V_{OUT} = 0.8 \cdot (1 + \frac{R1}{R2}) \qquad (V)$$

Suggested R2 is in the range from 1K to 20kΩ. For portable applications, a 10k resistor is suggested for R2. To prevent stray pickup, please locate resistors R1 and R2 close to APW7142.

Input Capacitor Selection

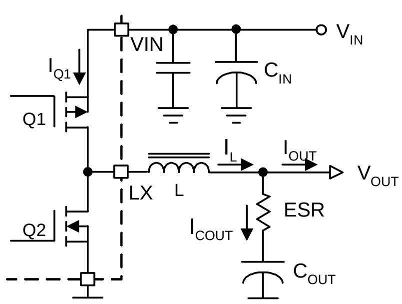
Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time the P-channel power MOSFET (Q1) turns on. Place the small ceramic capacitors physically close to the VIN and between the VIN and GND.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current (I_{RMS}) of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \qquad (A)$$

where D is the duty cycle of the power MOSFET.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.



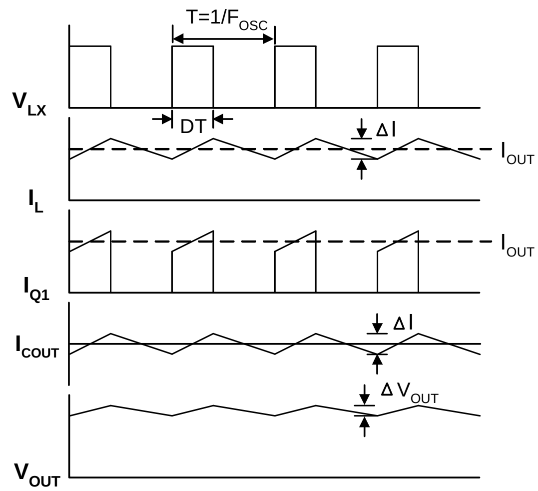


Figure 1 Converter Waveforms

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current (ΔI). The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calculated as the following equations:

$$D = \frac{V_{OUT}}{V_{IN}} \qquad \text{........... (1)}$$

$$\Delta I = \frac{V_{OUT} \cdot (1 - D)}{F_{OSC} \cdot L} \qquad \text{........... (2)}$$

$$V_{ESR} = \Delta I \cdot ESR \qquad \text{........... (3)}$$

The peak-to-peak voltage of the ideal output capacitor is calculated as the following equations:

$$\Delta V_{COUT} = \frac{\Delta I}{8 \cdot F_{OSC} \cdot C_{OUT}} \quad (V) \qquad \text{........... (4)}$$

For the applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is shown below:

$$\Delta V_{OUT} = \Delta I \cdot ESR \qquad (V) \qquad \text{........... (5)}$$

Application Information (Cont.)

Output Capacitor Selection (Cont.)

For the applications using ceramic capacitors, the V_{ESR} is much smaller than the ΔV_{COUT} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is close to ΔV_{COUT}.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses. The equation (2) shows that the inductance value has a direct effect on ripple current.

Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I \leq 0.4x\ I_{OUT(MAX)}$. Remember, the maximum ripple current occurs at the maximum input voltage. The minimum inductance of the inductor is calculated by using the following equation:

$$\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{500000 \cdot L \cdot V_{IN}} \leq 1.2$$

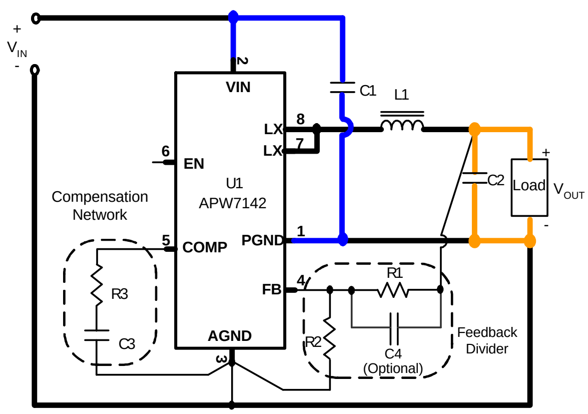
$$L \geq \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{600000 \cdot V_{IN}} \quad \text{(H)} \quad \text{........... (6)}$$

where $V_{IN} = V_{IN(MAX)}$

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 2 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Firstly, to initial the layout by placing the power components. Orient the power circuitry to achieve a clean power flow path. If possible, make all the connections on one side of the PCB with wide, copper filled areas.



2. In Figure 2, the loops with same color bold lines conduct high slew rate current. These interconnecting impedances should be minimized by using wide, short printed circuit traces.

3. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX or others) on the PCB. Therefore place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the AGND pin of the IC using a dedicated ground trace.

4. Place the decoupling ceramic capacitor C1 near the VIN as close as possible. Use a wide power ground plane to connect the C1 and C2 to provide a low impedance path between the components for large and high slew rate current.

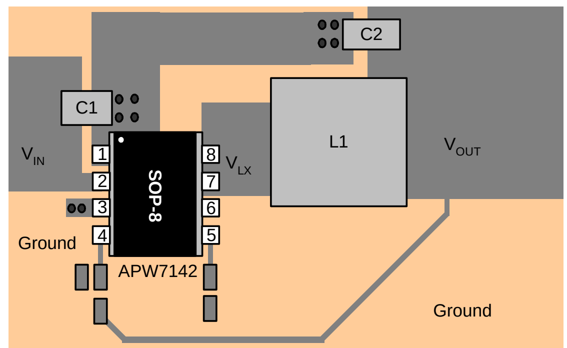
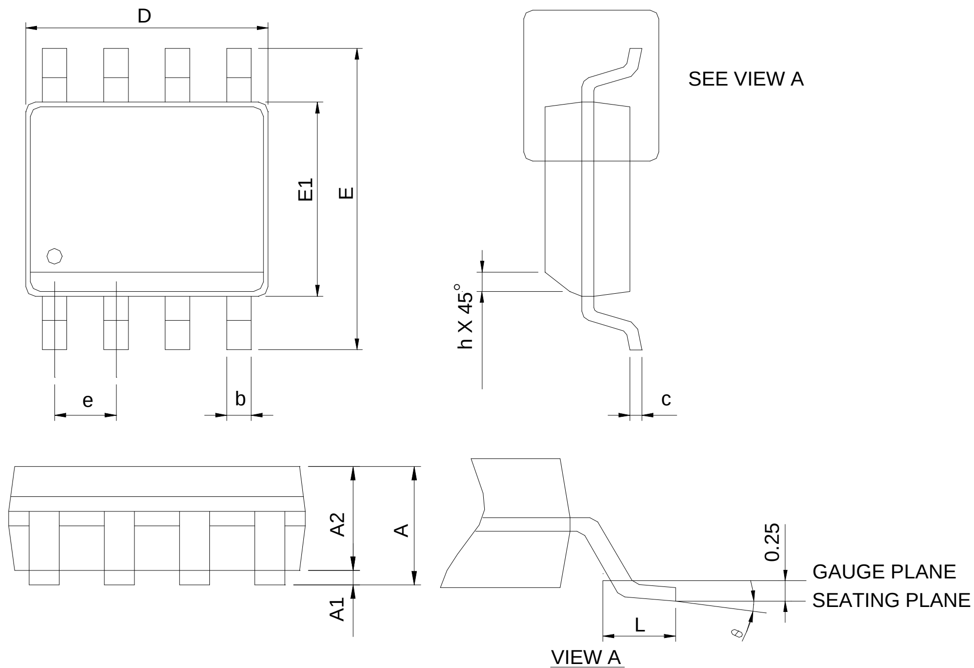


Figure 3 Recommended Layout Diagram

Package Information

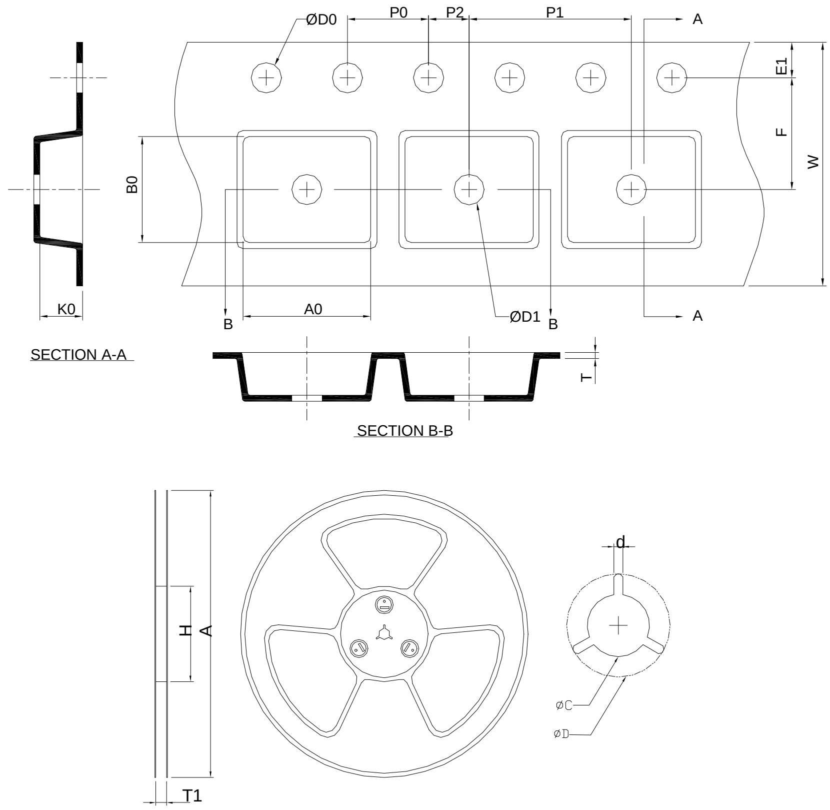
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



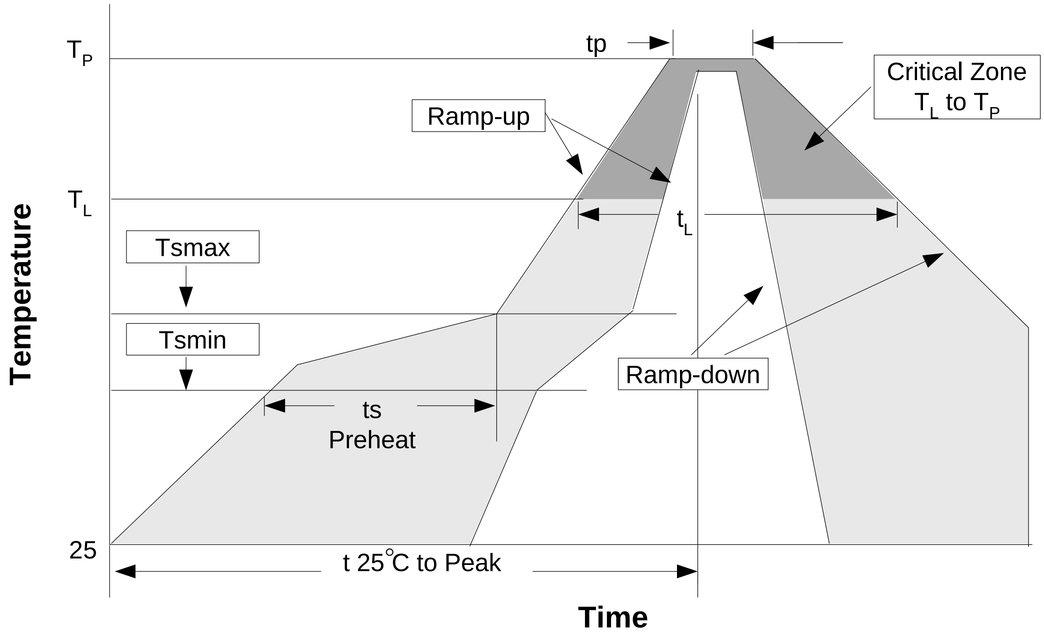
Application	A	H	T1	C	d	D	W	E1	F
SOP-8(P)	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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