

# Video Signal Driver for DVD Players

## Monolithic IC MM1566

October 25, 2001

### Outline

This IC is a video signal driver IC that supports 3-ch interlace video developed for DVD players. It includes a low-pass filter that attenuates the noise element during DA conversion, and a 3-channel 6dB amp with 75Ω driver.

In addition, external ESD protection diodes can be reduced by a sag correction pin for reducing output coupling capacitance, and enhancement of the ESD protection elements for the output pins.

### Features

1. Includes a SAG correction pin.
2. Enabled to drive a 3-channel 6dB amp with 75Ω driver
3. Includes a 4th-order low-pass filter  
Frequency response: 6.75MHz ± 1dB / 27MHz – 27dB min.
4. Includes a 6dB amp
5. Includes a power save function
6. S/N=80dB typ. (Y/C mix:74dB typ.)
7. ESD strength (aerial discharge) of ±15kV (IEC standard)
8. Includes mode select pins which correspond to various video signals

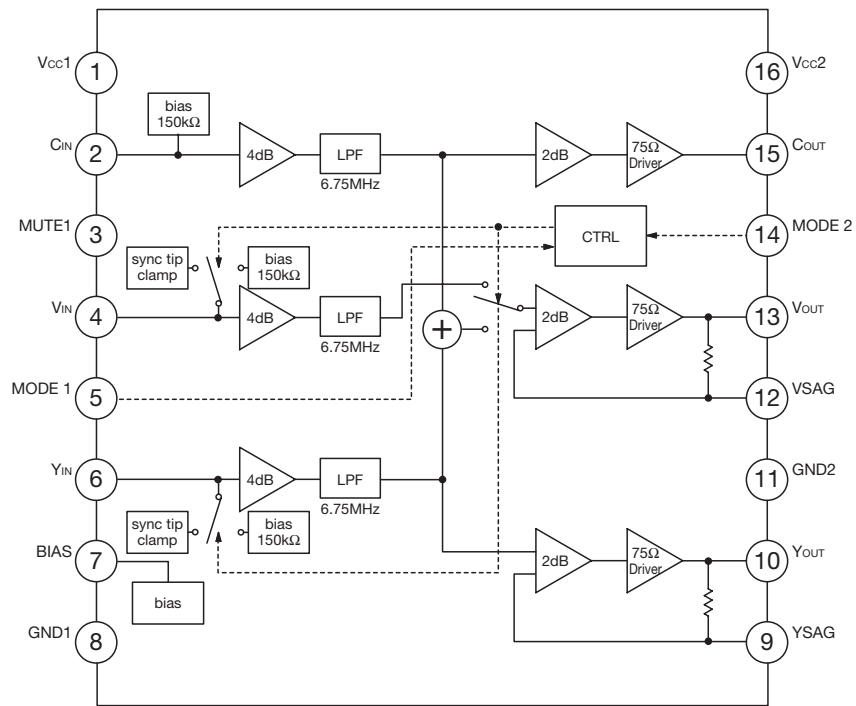
### Package

SOP-16C

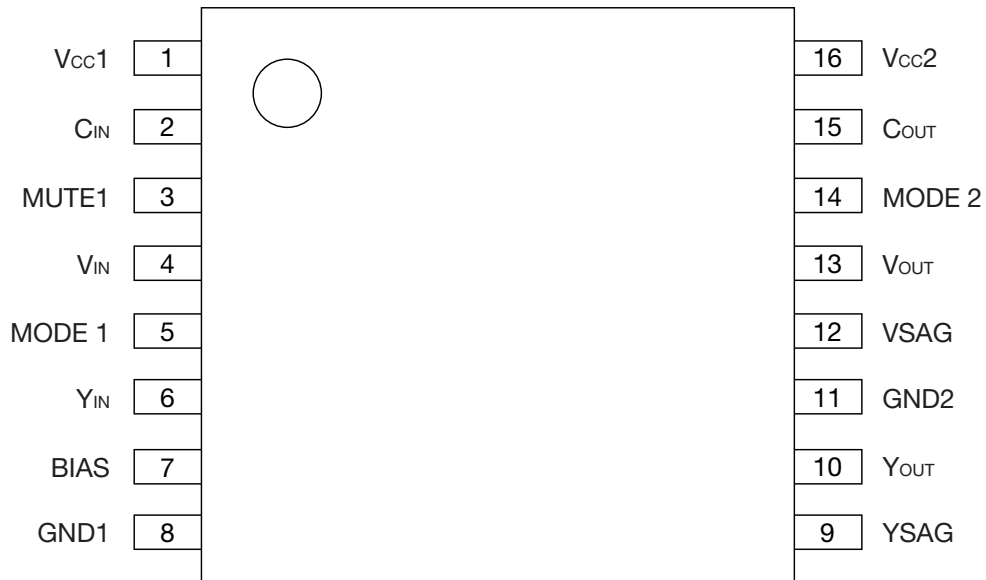
### Applications

- (1)DVD players
- (2)Digital STB
- (3)Other digital video equipment

Block diagram



Pin Assignment



SOP-16C

1	Vcc1	9	YSAG
2	C <sub>IN</sub>	10	Y <sub>OUT</sub>
3	MUTE1	11	GND2
4	V <sub>IN</sub>	12	VSAG
5	MODE 1	13	V <sub>OUT</sub>
6	Y <sub>IN</sub>	14	MODE 2
7	BIAS	15	C <sub>OUT</sub>
8	GND1	16	Vcc2

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 16	V <sub>CC1</sub> V <sub>CC2</sub>	V <sub>CC</sub>	
2	C <sub>IN</sub>	Croma input	
3	MUTE1	Mute select  Using of MUTE and POWER-SAVING.	
4 6	V <sub>IN</sub> Y <sub>IN</sub>	Video input  The input can select Sync tip clamp or Bias	
5 14	MODE1 MODE2	Mode select	

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7	BIAS	Bias	
8 11	GND1 GND2	GND	
10 13		Signal output	
9 12		SAG correction	
15	Cout	Croma output	

### Absolute Maximam Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Storage temperature	T <sub>STG</sub>	-65 ~ +150	°C
Operating temperature	T <sub>OPR</sub>	-40 ~ +85	°C
Supply Voltage	V <sub>CC</sub> max.	7	V
Power dissipation *1	P <sub>d</sub>	1.0	W

note \*1 Board mounting power dissipation. Board size 21.3mmX38.1mmX1.0mm

### Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating temperature	T <sub>OPR</sub>	-40 ~ +85	°C
Operating Voltage	V <sub>CCOP</sub>	4.5 ~ 5.5	V

### Electrical Characteristics (Unless otherwise specified, Ta=25°C, Vcc=5V)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Consumption current 1	I <sub>CC1</sub>	No signal	39	55	71	mA
Consumption current 2	I <sub>CC2</sub>	No signal Mute1:ON	1	3	5	mA
Bias input	V <sub>INbias</sub>	at Bias select	1.9	2.4	2.9	V
Clamp input	V <sub>INclamp</sub>	at Clamp select	1.15	1.4	1.65	V
Bias output	V <sub>OUTbias</sub>	at Bias select		2.4		V
Clamp output	V <sub>OUTclamp</sub>	at Clamp select		1.1		V
Control terminal input current	H	I <sub>IHm</sub> *2			350	μA
	L	I <sub>IL</sub> *2			35	μA
Control terminal input voltage	H	V <sub>thHm</sub> *2	2.1			V
	L	V <sub>thLm</sub> *2			0.7	V
Input impedance	Z <sub>INbias</sub>	at Bias select	100	150	200	kΩ
Voltage gain	G <sub>n</sub> *3	S <sub>IN</sub> wave:1V f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic 1	f <sub>1n</sub> *3	S <sub>IN</sub> wave:1V 6.75MHz/100kHz	-1.0	0	1.0	dB
Frequency characteristic 2	f <sub>2n</sub> *3	S <sub>IN</sub> wave:1V 27MHz/100kHz		-40	-27	dB
Differential gain	DG <sub>1~3</sub> *3	Staircase signal 1V		0.6	1.0	%
Differential phase	DP <sub>1~3</sub> *3	Staircase signal 1V		0.6	1.0	°
Output dynamic range	DR <sub>n</sub> *3	S <sub>IN</sub> wave:100kHz THD=1.0%	2.6	3.0		V
Crosstalk	CT <sub>n</sub> *3	f=4.43MHz, 1V		-60	-55	dB
S/N 1	SN <sub>14,5</sub> *3	BW:100k ~ 6MHz		-80		dB
S/N 2	SN <sub>21~3</sub> *3	BW:100k ~ 6MHz at MIX OUT		-74		dB
Group delay	t <sub>GDn</sub> *3	at 100kHz		50		ns
Group delay deviation	Δt <sub>GDn</sub> *3	to 3.58MHz		4		ns
		to 4.43MHz		7		ns
		to 6MHz		12		ns

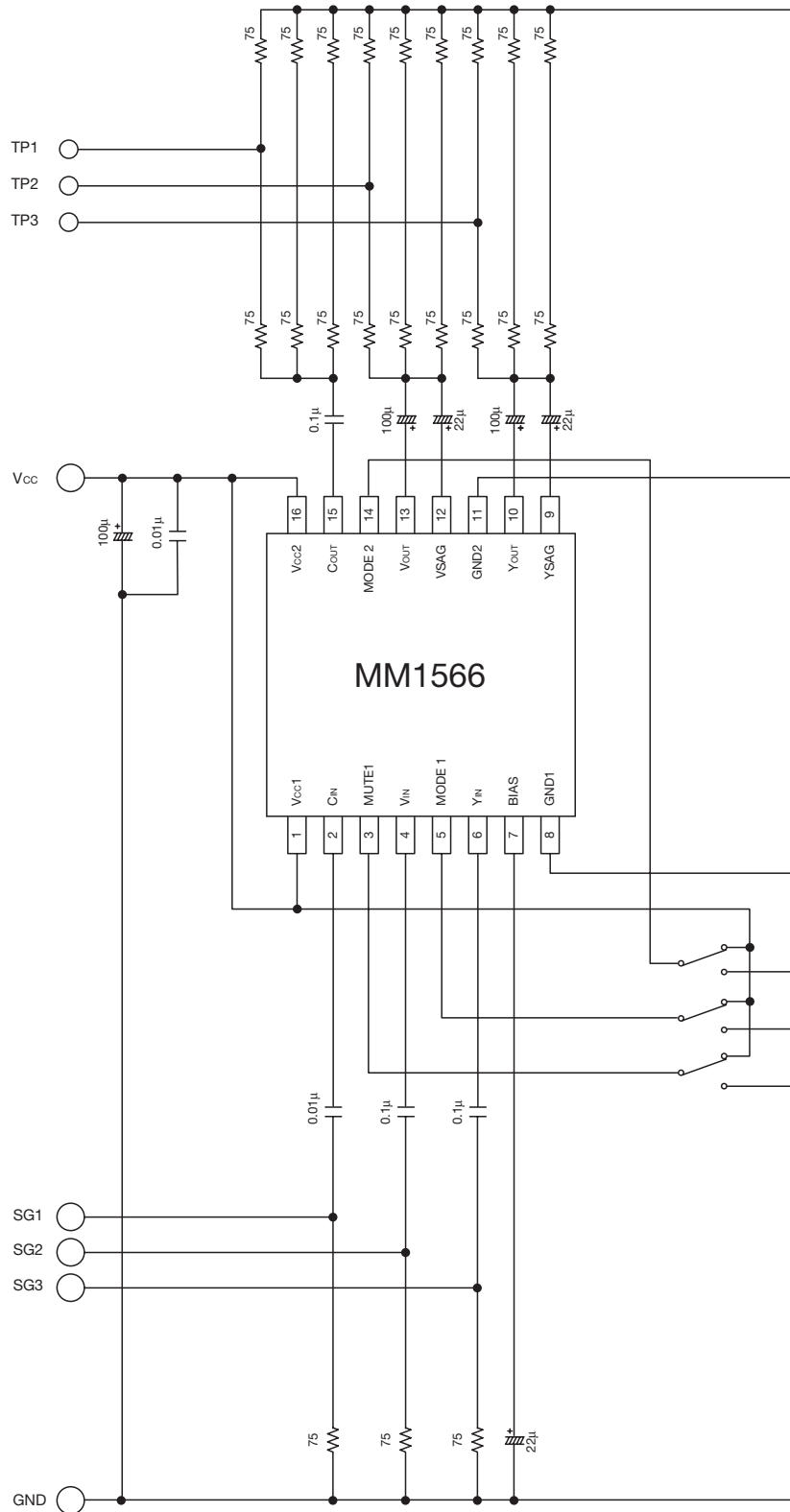
note \*2 The subscript number "m" is the terminal of right table.

note \*3 The subscript number "n" is the combination of right table.

m	Terminal
1	MUTE1
2	MODE1
3	MODE2

n	Input	Output
1	C <sub>IN</sub>	V <sub>OUT</sub>
2	V <sub>IN</sub>	
3	Y <sub>IN</sub>	
4	C <sub>IN</sub>	C <sub>OUT</sub>
5	Y <sub>IN</sub>	Y <sub>OUT</sub>

Measuring Circuit

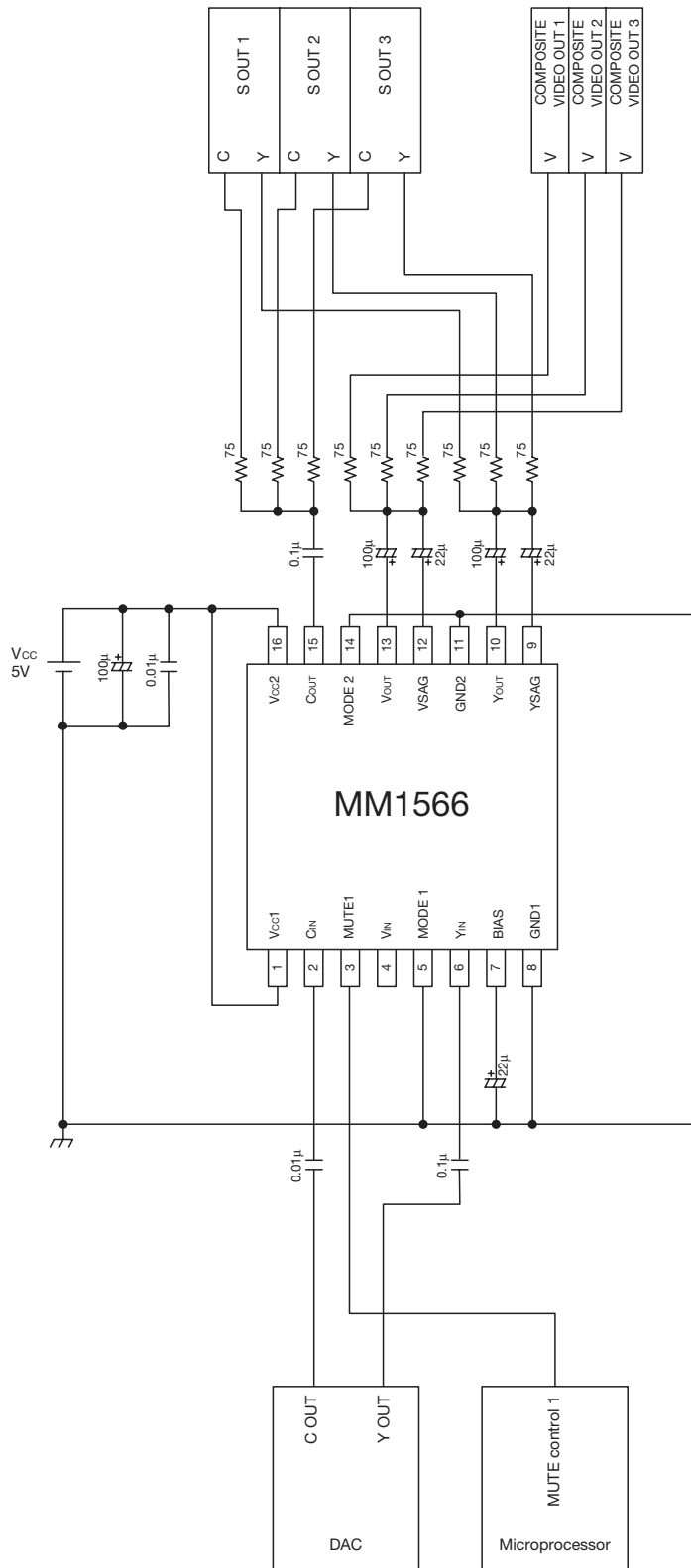


**Switch Control Table**

	Input Terminal	Input Signal (Input clamp)	Output Signal	Control Terminal		
				MUTE1	MODE1	MODE2
<b>1</b>	MUTE	*	MUTE	Low	*	*
	C <sub>IN</sub>	C(bias)	C	High	Low	Low
	V <sub>IN</sub>		Composite Video(Y+C)			
	Y <sub>IN</sub>	Y(clamp)	Y			
<b>2</b>	MUTE	*	MUTE	Low	*	*
	C <sub>IN</sub>	C(bias)	C	High	High	Low
	V <sub>IN</sub>	Composite Video(clamp)	Composite Video			
	Y <sub>IN</sub>	Y(clamp)	Y			
<b>3</b>	MUTE	*	MUTE	Low	*	*
	C <sub>IN</sub>	Cr(bias)	Cr	High	Low	High
	V <sub>IN</sub>	Cb(bias)	Cb			
	Y <sub>IN</sub>	Y(clamp)	Y			
<b>4</b>	MUTE	*	MUTE	Low	*	*
	C <sub>IN</sub>	R(bias)	R	High	High	High
	V <sub>IN</sub>	G(bias)	G			
	Y <sub>IN</sub>	B(bias)	B			

\* : Don't care

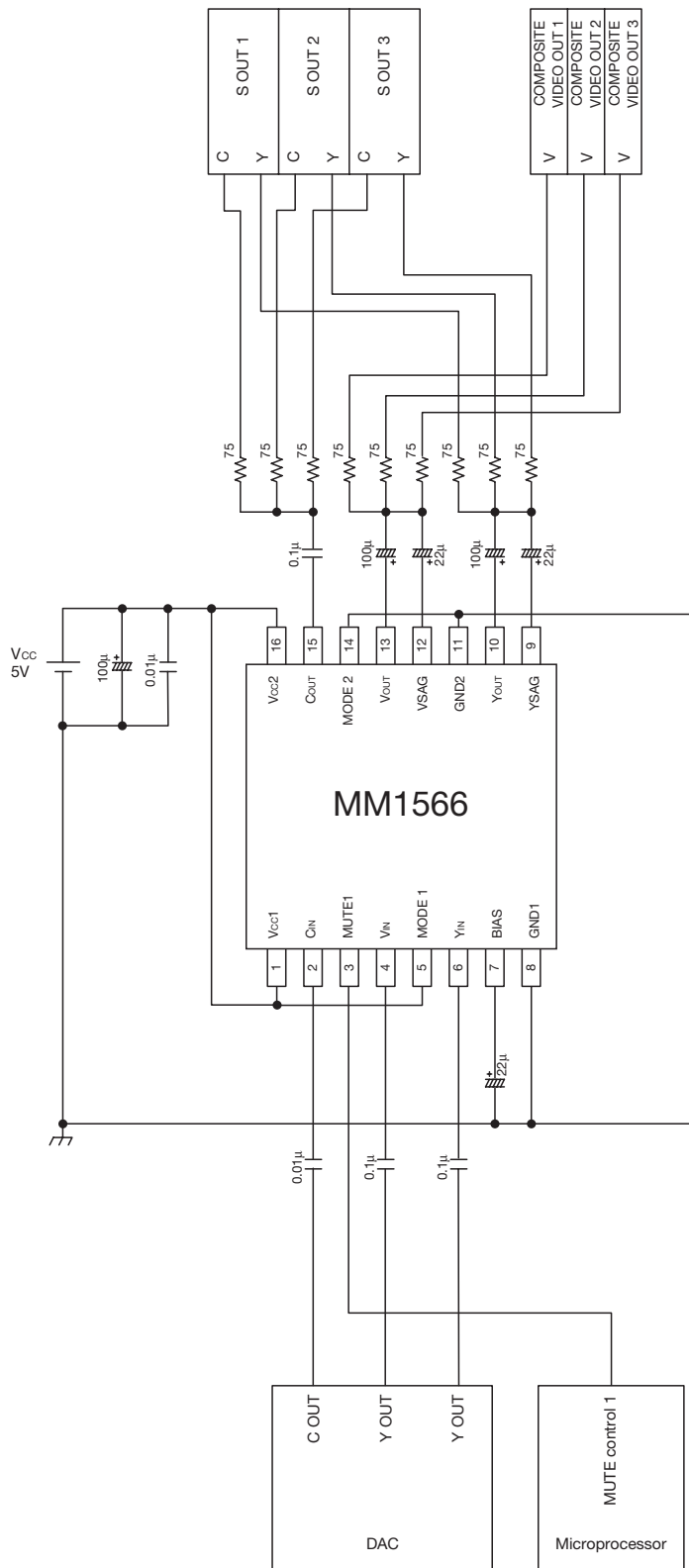
Application Circuit 1



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

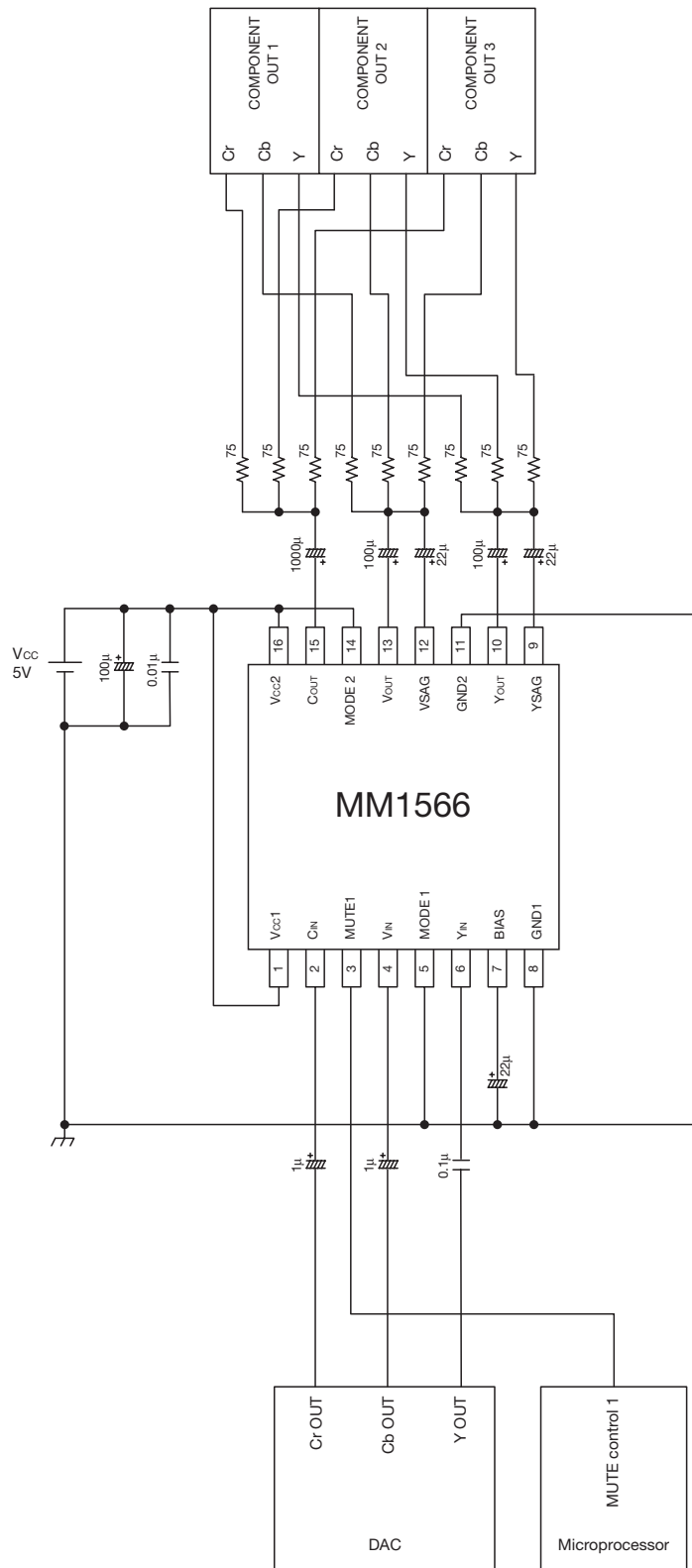


Application Circuit 2



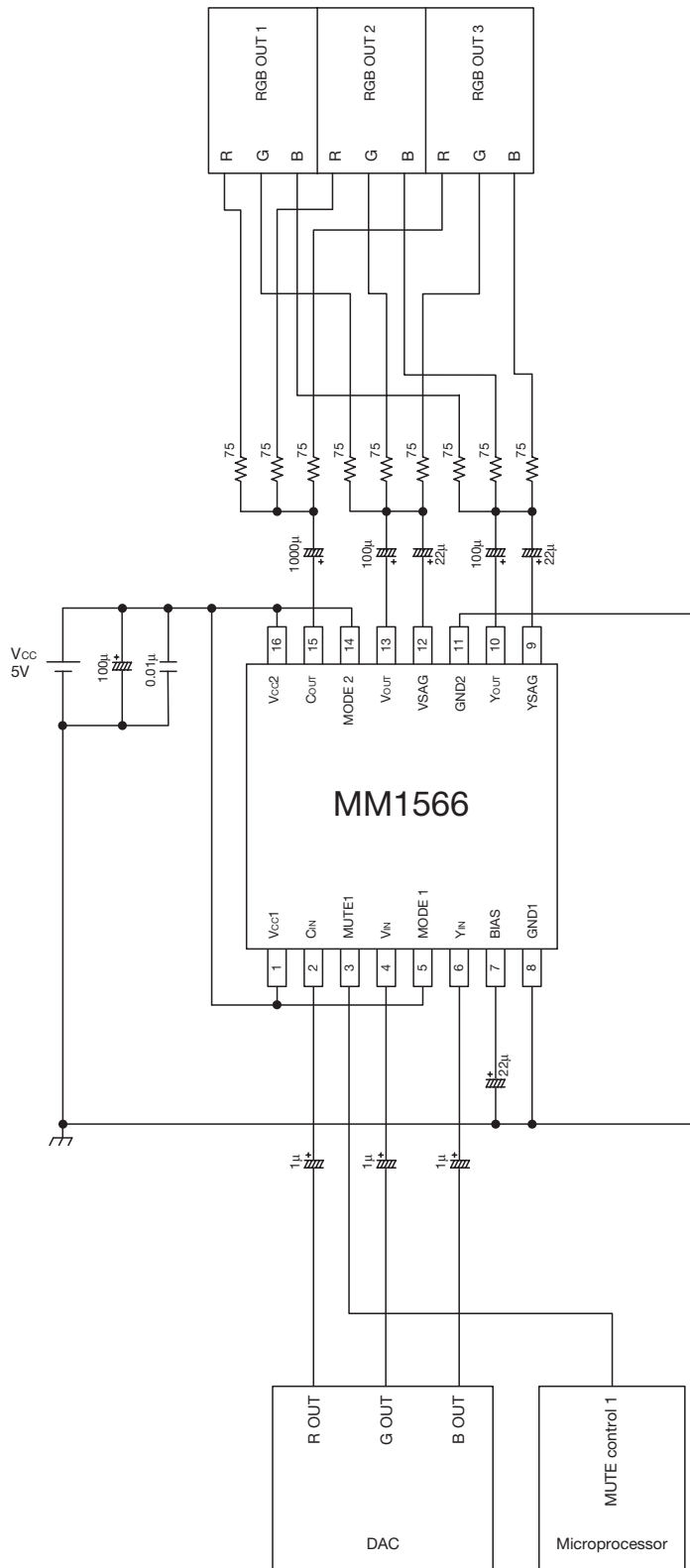
(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

Application Circuit 3



(note) : Please arrange power supply bypass capacitor near the V<sub>CC2</sub> terminal (16PIN).

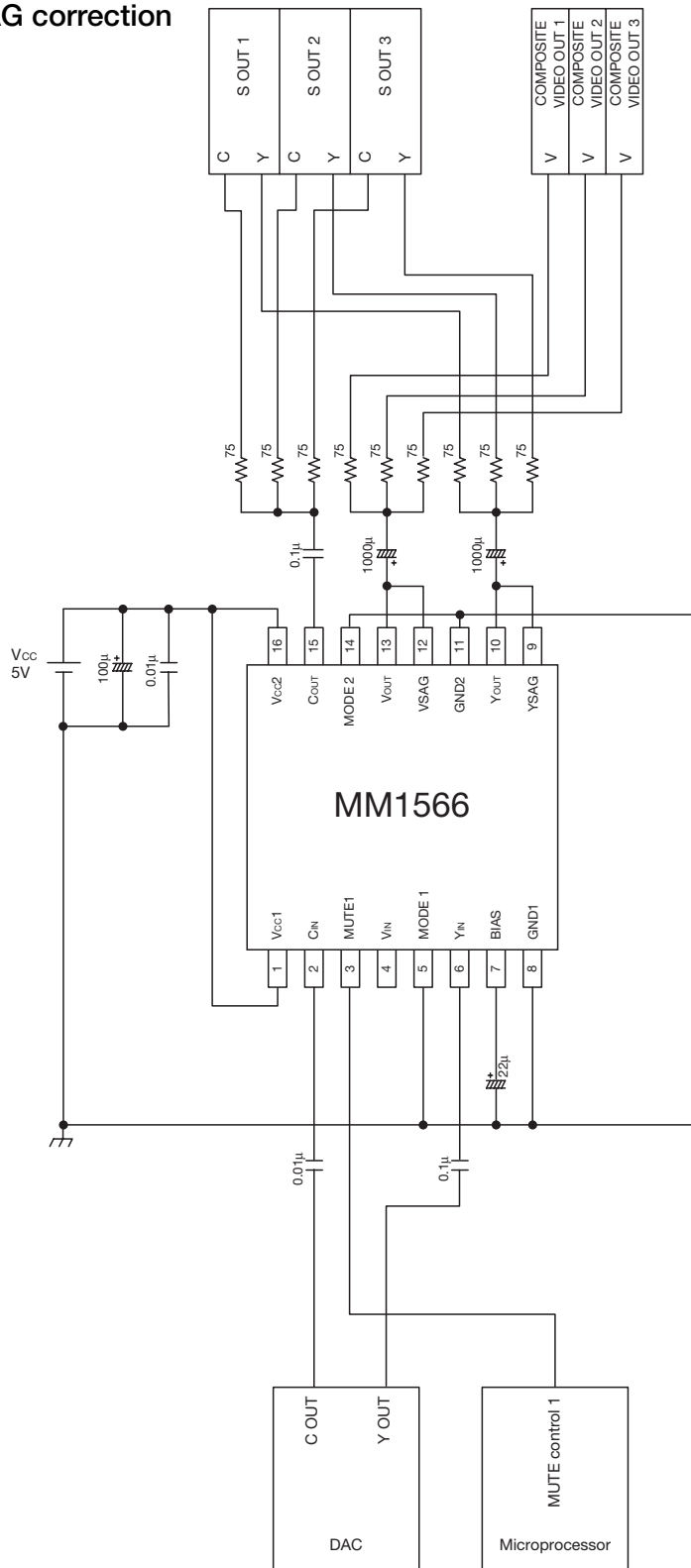
Application Circuit 4



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

Application Circuit 5

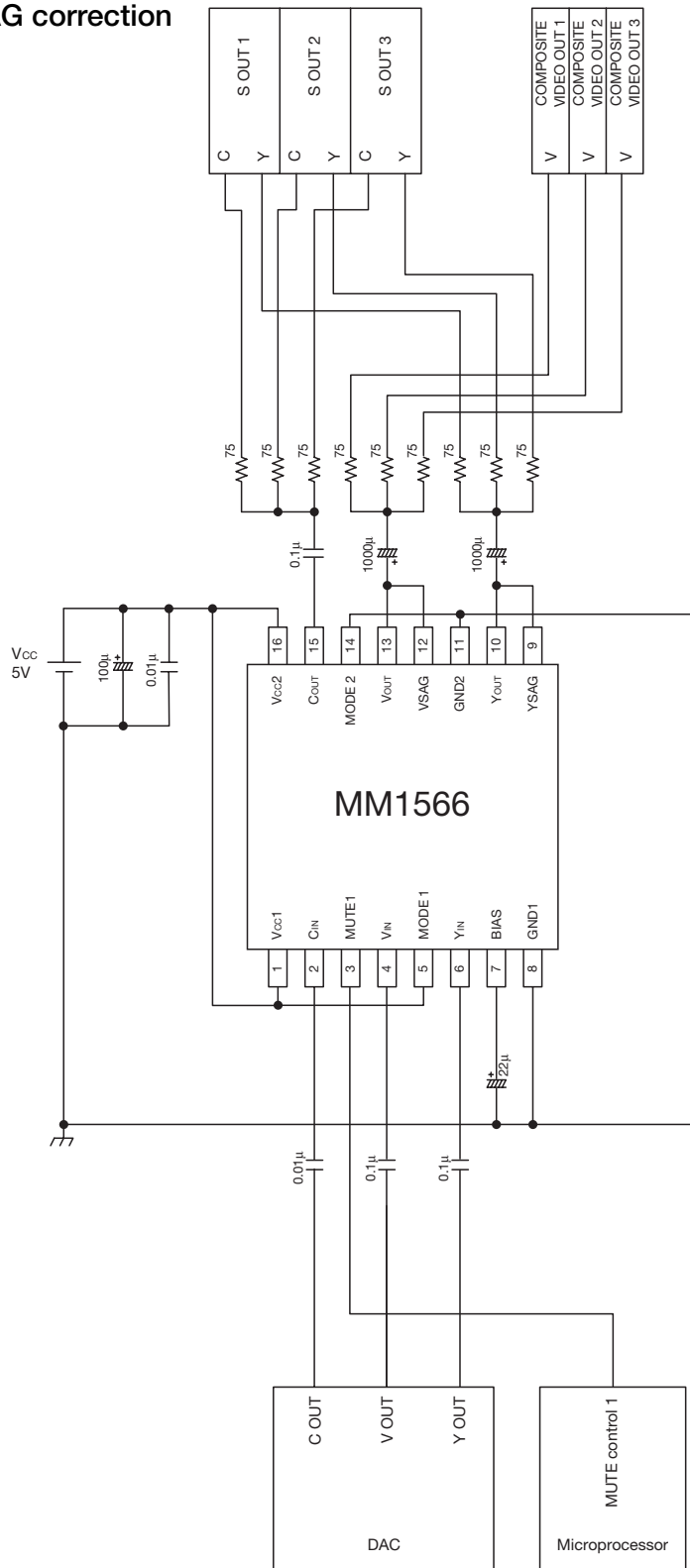
■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

Application Circuit 6

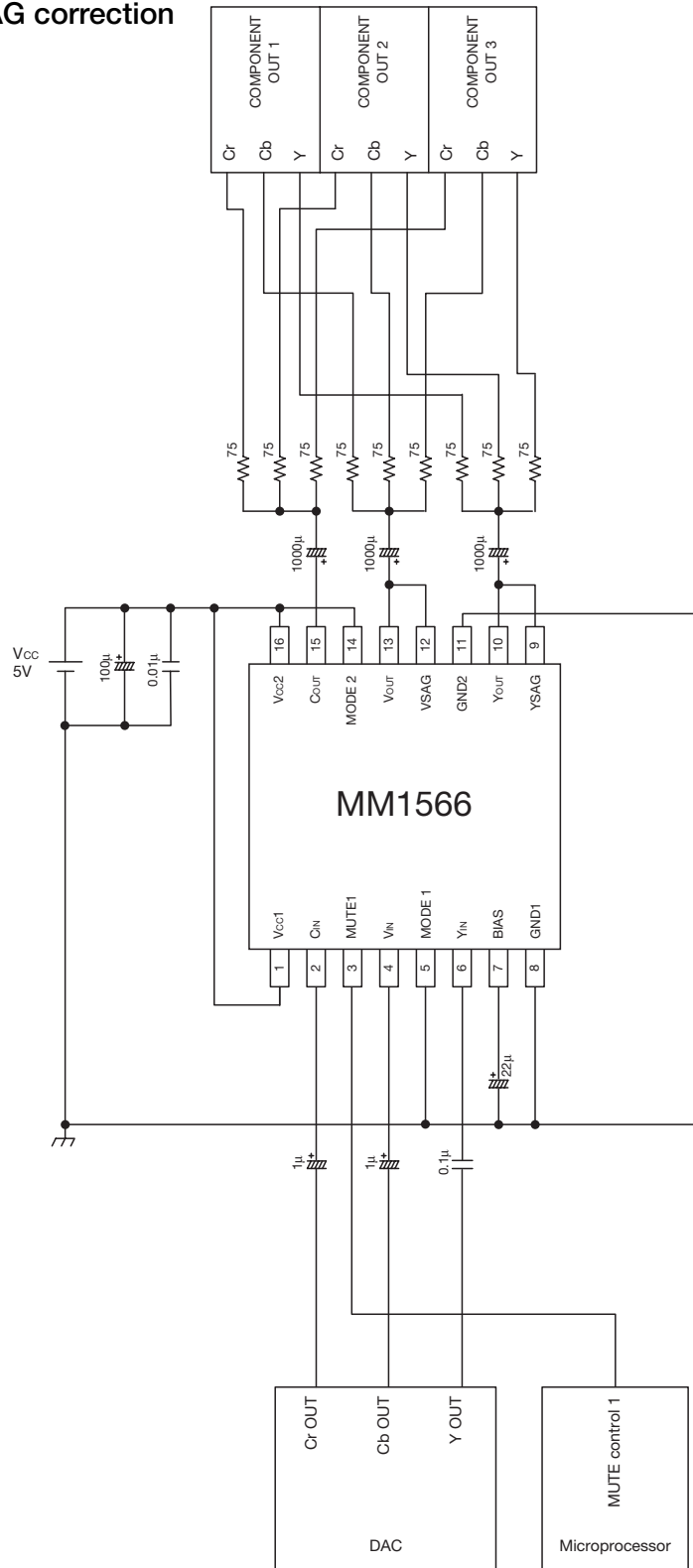
■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

Application Circuit 7

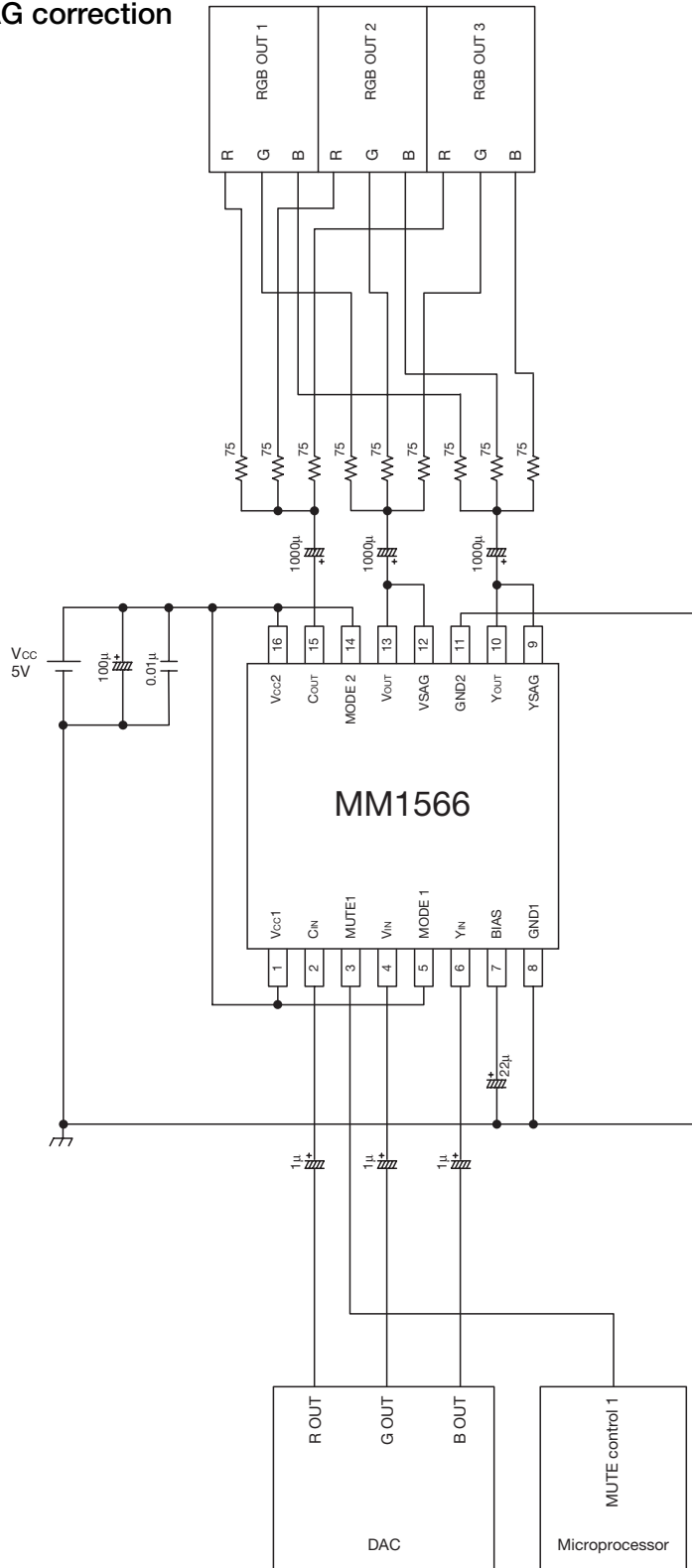
■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).

Application Circuit 8

■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (16PIN).