

Audio Accessory IC Series



Band-pass Filter for Spectrum Analyzer Indication

BA3835F, BA3830F, BA3834F

●Description

As BA3835F, BA3830F, and BA3834F contain band pass filters for spectrum analyzer, external mount parts can be significantly reduced enabling compact unit size and high reliability.

●Features

- 1) Built-in band pass filter for spectrum analyzer. BA3835F has 5 bands filters, BA3830F has 6 bands filters, and BA3834F has 7 bands filters.
- 2) BA3834F and BA3835 have an integrated multiplexer circuit. Controlled by a microcontroller, detection level is serially output with DC level.
- 3) BA3830F output for recording indicator. Detection level is parallel output in DC.
- 4) Support 5V microcomputer bus
- 5) SOP18 package with few external parts

●Applications

Car audio, mini audio stereo systems, and CD radio cassette players.

●Product lineup

Item	BA3835F	BA3830F	BA3834F
Number of Band	5	6	7
Center frequency of the band pass filter (Hz)	105,340,1K,3.4K,10.5K	63,150,330,1K,3.3K,10K	68,170,420,1K,2.4K,5.9K,14.4K
Power voltage (V)	4.5~6.5	4.5~8	4.5~6.5
Output type	Serial output	Parallel output	Serial output
Working temperature range (°C)	-25 ~ +75	-25 ~ +75	-25 ~ +75
Package	SOP18	SOP18	SOP18

● **Absolute maximum ratings** (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage	BA3834F,BA3835F	Vcc	7	V
	BA3830F		9	
Power dissipation		Pd	450*	mW
Operating temperature		Topr	-25~+75	°C
Storage temperature		Tstg	-55~+125	°C

* Reduced by 4.5 mW/°C over 25°C

● **Recommended operating conditions** (Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	BA3834F,BA3835F	Vcc	4.5	5.0	6.5	V
	BA3830F		4.5	—	8.0	

● **Electrical characteristics**

BA3835F (unless otherwise noted, Ta=25°C, VCC=5V, RL=10MΩ, VAIN=−30dBV, SEL=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current	ICC	—	8.5	13	mA	VAIN = 0V, A, B, C, SEL = 0
Maximum output level	VOM	4.0	4.8	—	V	VAIN = -14dBV, Measured at each output
Output offset voltage	VOS	—	30	150	mV	VAIN = 0V, SEL = 0/1 Measured at each output (cycle time : Ts=50ms)
Standard output level 1	V01	0.65	1.35	1.70	V	fIN =105Hz, A=0, B=0, C=1
Standard output level 2	V02	0.65	1.35	1.70	V	fIN =340Hz, A=0, B=1, C=0
Standard output level 3	V03	0.65	1.35	1.70	V	fIN =1kHz, A=1, B=0, C=0
Standard output level 4	V04	0.65	1.35	1.70	V	fIN =3.4kHz, A=1, B=1, C=0
Standard output level 5	V05	0.65	1.35	1.70	V	fIN =10.5kHz, A=1, B=1, C=1
Input impedance	RIN	80	100	120		fIN =1kHz
Common-mode rejection ratio	CMRR	25	50	—	dB	fIN =1kHz, VAIN =VCIN
Logic input high level	VIH	2.5	5.0	—	V	
Logic input low level	VIL	—	0	0.5	V	Not Applicable in the when item 3 of the operation notes applies.
Output response time*1	TO	—	5	10	μs	
Discharge level	DL	—	3	—	dB	Reset pulse within TR=10 μs (Typ.)*2

*1 The time from the rise of A, B, C or SEL until the rise of AOOUT (90% of peak). If the output selection time is less than this, the output value is not guaranteed and the reset pulse is not generated.

*2 Automatically generated internally based on the output select signal. For the duration that this signal is "H", a resistor is connected to the peak hold capacitor, and the output level drops by -3dB (typ.) for one pluse,

*3 The Q of the bandpass filter is 3.5.

© Not designed for radiation resistance.

BA3830F (unless otherwise noted, Ta=25°C, V_{CC}=5V, R_L=10MΩ, R_{φ1}=270kΩ, R_{φ2}=270kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I _O	—	3.8	5.2	mA	
Reference output level (LEVEL)	V _{ol}	-3	0	3	dB	V _{IN} = -30dBV, V _O = 1.5V (0dB) When f = center frequencies is input
Max. output level (LEVEL)	V _{olmax}	3.2	4.2	—	V	V _{IN} = -14dBV, When f = center frequencies is input
Reference output level (REC LEVEL)	V _{or}	-3	0	3	dB	V _{IN} = -30dBV, V _O = 1.5V (0dB) f = 1kHz
Max. output level (REC LEVEL)	V _{olmax}	3.8	4.8	—	V	V _{IN} = -14dBV, f = 1kHz
Output offset voltage	V _{off}	—	30	90	mV	With no signal
Center frequency 1	f ₀₁	49	63	77	Hz	V _{IN} = -30dBV
Center frequency 2	f ₀₂	117	150	183	Hz	V _{IN} = -30dBV
Center frequency 3	f ₀₃	257	330	403	Hz	V _{IN} = -30dBV
Center frequency 4	f ₀₄	0.78	1	1.22	kHz	V _{IN} = -30dBV
Center frequency 5	f ₀₅	2.55	3.3	4.03	kHz	V _{IN} = -30dBV
Center frequency 6	f ₀₆	7.8	10	12.2	kHz	V _{IN} = -30dBV
Input current when Reset pin is HIGH	I _{IN}	150	215	280	μA	V _{IN} = 5V
Input current when Reset pin is ON	V _{th}	—	1.4	1.8	V	
Input current when Reset pin is OFF	V _{th}	1.0	1.4	—	V	

* Q is set to 4.5.

⊙ Not designed for radiation resistance.

BA3834F (unless otherwise noted, Ta=25°C, V_{CC}=5V, R_L=10MΩ, V_{AIN}=-30dBV, SEL=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current	I _{CC}	—	10	15	mA	V _{AIN} = 0V, A, B, C, SEL=0
Maximum output level	V _{OM}	4.0	4.8	—	V	V _{AIN} = -14dBV, Measured at each output
Output offset voltage	V _{OS}	—	30	150	mV	V _{AIN} = 0V, SEL=0/1, Measured at each output (cycle time : Ts=50ms)
Standard output level 1	V ₀₁	0.65	1.35	1.70	V	f _{IN} = 68Hz, A=0, B=0, C=1
Standard output level 2	V ₀₂	0.65	1.35	1.70	V	f _{IN} = 170Hz, A=0, B=1, C=0
Standard output level 3	V ₀₃	0.65	1.35	1.70	V	f _{IN} = 420Hz, A=0, B=1, C=1
Standard output level 4	V ₀₄	0.65	1.35	1.70	V	f _{IN} = 1kHz, A=1, B=0, C=0
Standard output level 5	V ₀₅	0.65	1.35	1.70	V	f _{IN} = 2.4kHz, A=1, B=0, C=1
Standard output level 6	V ₀₆	0.65	1.35	1.70	V	f _{IN} = 5.9kHz, A=1, B=1, C=0
Standard output level 7	V ₀₇	0.65	1.35	1.70	V	f _{IN} = 14.4kHz, A=1, B=1, C=1
Input impedance	R _{IN}	80	100	120	Ω	f _{IN} = 1kHz
Common-mode rejection ratio	CMRR	25	50	—	dB	f _{IN} = 1kHz, V _{AIN} = V _{CIN}
Logic input high level	V _{IH}	2.5	5.0	—	V	
Logic input low level	V _{IL}	—	0	0.5	V	Not Applicable in the when item 3 of the operation notes applies.
Output response time* ¹	T _O	—	5	10	μs	
Discharge level	DL	—	3	—	dB	Reset pulse within T _R = 10 μs (Typ.)* ²

*1 The time from the rise of A, B, C or SEL until the rise of AOUT (90% of peak). If the output selection time is less than this, the output value is not guaranteed and the reset pulse is not generated.

*2 Automatically generated internally based on the output select signal. For the duration that this signal is "H", a resistor is connected to the peak hold capacitor, and the output level drops by -3dB (typ.) for one pulse,

*3 The Q of the bandpass filter is 3.5 for f₀₁ to f₀₆, and 2.5 for f₀₇.

⊙ Not designed for radiation resistance.

●Application example (BA3835F)

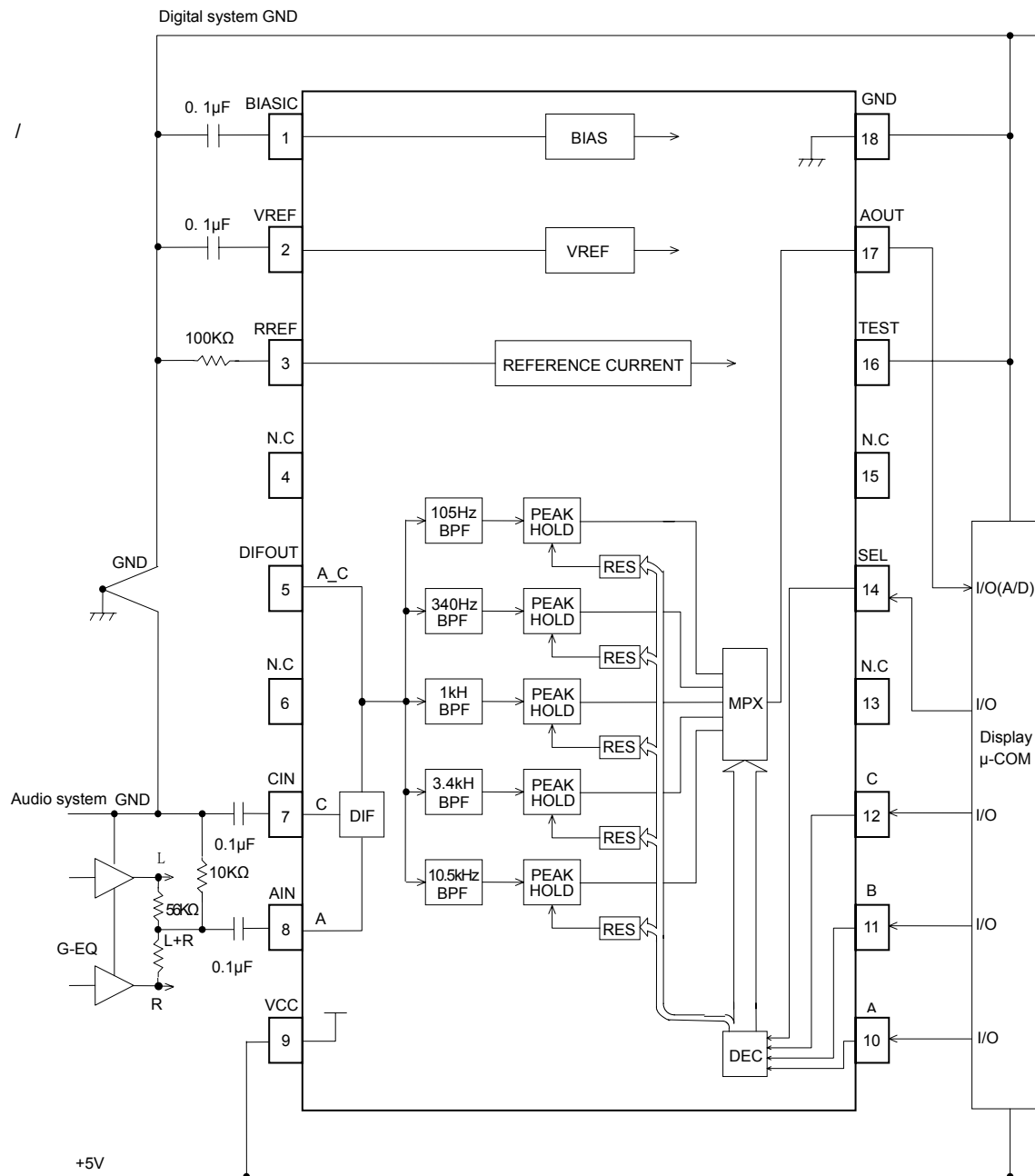


Fig.1

●Application example (BA3835F)

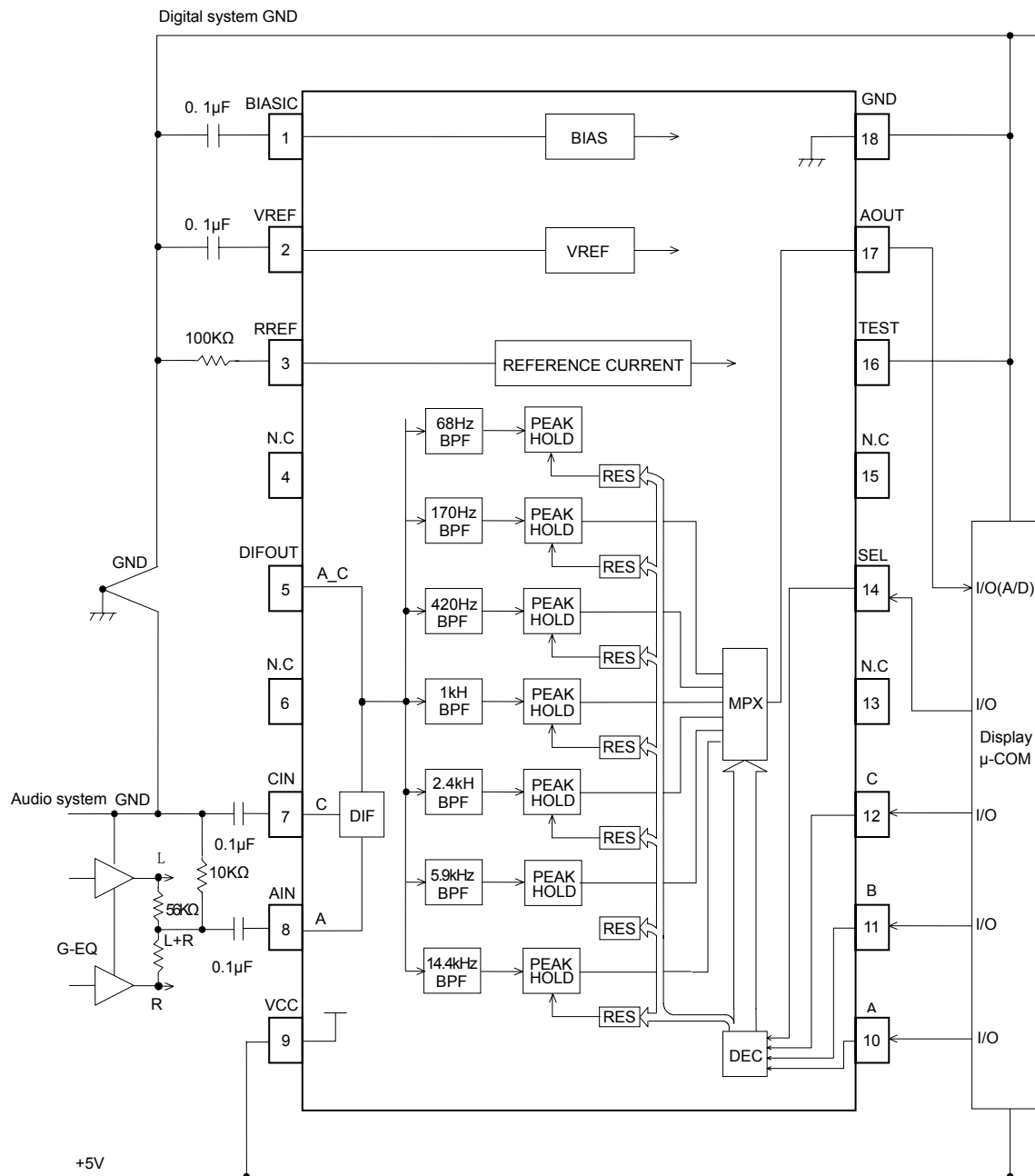


Fig.1

●Application example (BA3830F)

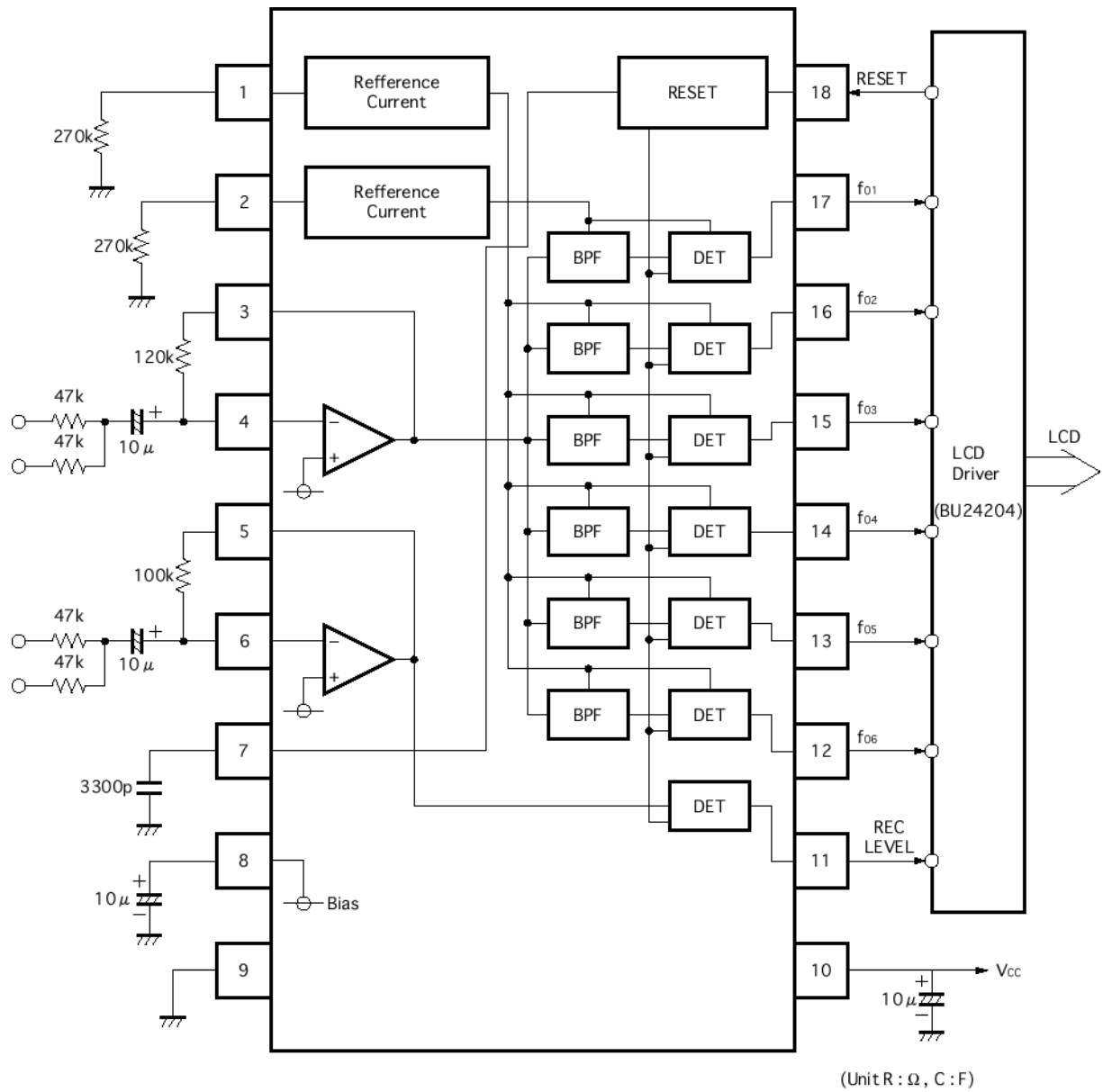


Fig.3

●Electrical characteristics curves

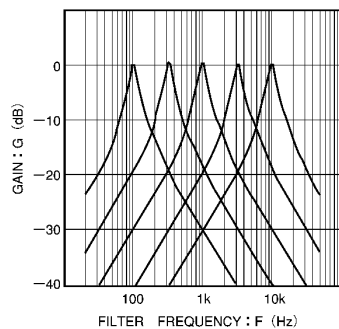


Fig.4 BPF frequency characteristics (BA3835F)

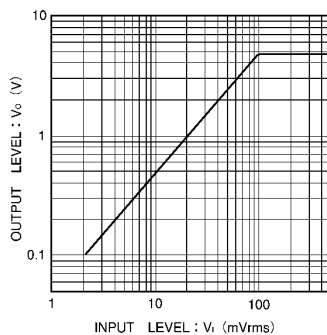


Fig.5 Input level vs. output level (BA3835F)

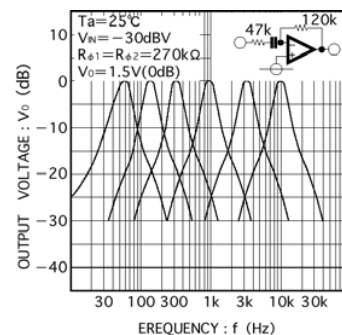


Fig.6 Output vs. frequency (BA3830F)

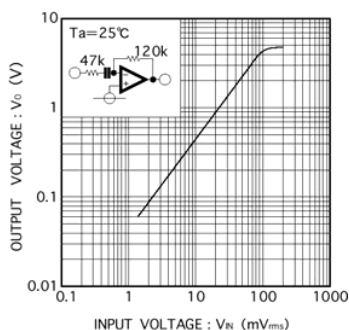


Fig.7 Input vs. output level (BA3830F)

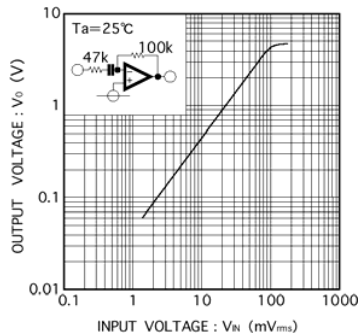


Fig.8 Input vs. output level (BA3830F REC mode)

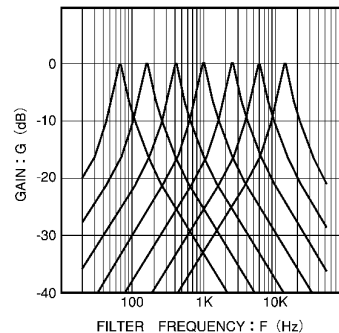


Fig.9 BPF frequency characteristics (BA3834F)

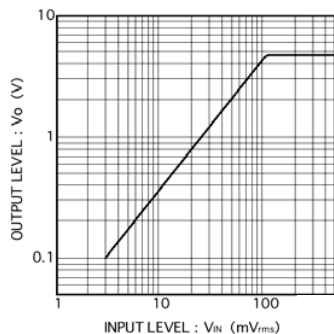
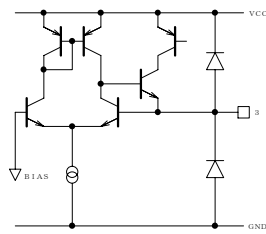
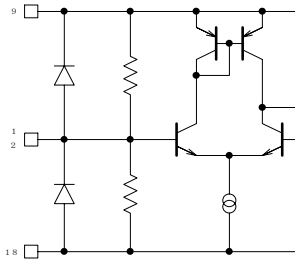


Fig.10 Input level vs. output level (BA3834F)

● Terminal explanation (BA3834F,BA3835F)

Terminal No.	Terminal name	Terminal Explanation	I/O Circuit Diagram
10	A	Output selection control terminal (Refer to the output selection logic table)	
11	B		
12	C		
14	SEL		
16	TEST	Test signal input terminal must be connect to GND.	
4, 6 13, 15	N.C.	Terminal not used	
5	DIFOUT	Differential amplifier output terminal Open for proper use	
7	CIN	Differential amplifier input terminal2 Connect capacitor to GND for audio signals.	
8	AIN	Differential amplifier input terminal1 Input audio signal through coupling capacitor.	
17	AOUT	Multiplex output terminal Select one band out of 5 or 7 bands. Peak hold voltage is output. After selection, reset pulse will cause it to attenuate to -3dB level	

Terminal No.	Terminal name	Terminal Explanation	I/O Circuit Diagram
3	RREF	Setting of band pass filter Connect external adjustments. Reference resistor to terminal (for band shift only).	
2	VREFC	For logic voltage Decoupling capacitor connection terminal	
1	BIASC	For analog voltage Decoupling capacitor connection terminal	
9	VCC	Power supply terminal	
18	GND	Grounding terminal	

●Output select logic table (BA3835F)

SEL	A	B	C	AOUT
0	×	×	×	GND
1	0	0	0	GND
1	0	0	1	105Hz
1	0	1	0	340Hz
1	0	1	1	GND
1	1	0	0	1kHz
1	1	0	1	GND
1	1	1	0	3.4kHz
1	1	1	1	10.5kHz

×:Don't Care.

●Timing chart (BA3835F)

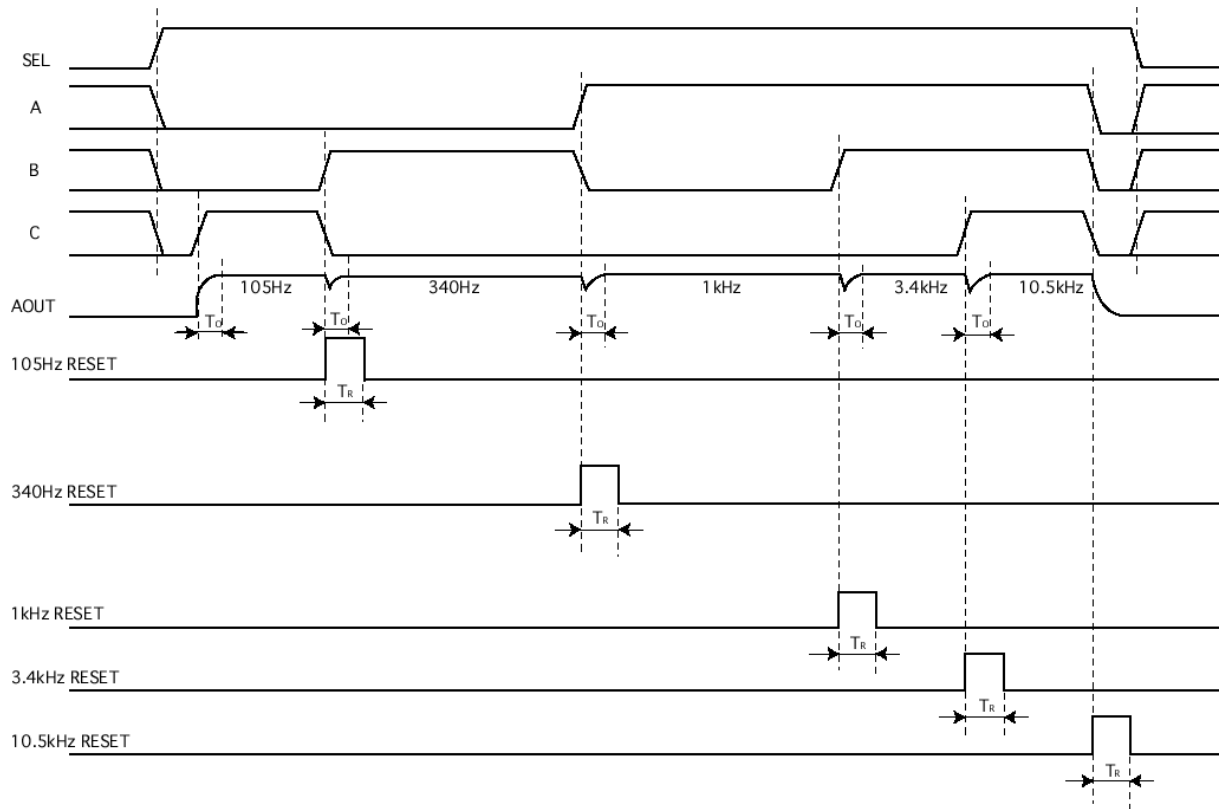


Fig.11

●Output select logic table (BA3834F)

SEL	A	B	C	AOUT
0	×	×	×	GND
1	0	0	0	GND
1	0	0	1	68Hz
1	0	1	0	170Hz
1	0	1	1	420Hz
1	1	0	0	1kHz
1	1	0	1	2.4kHz
1	1	1	0	5.9kHz
1	1	1	1	14.4kHz

×:Don't Care.

●Timing chart (BA3834F)

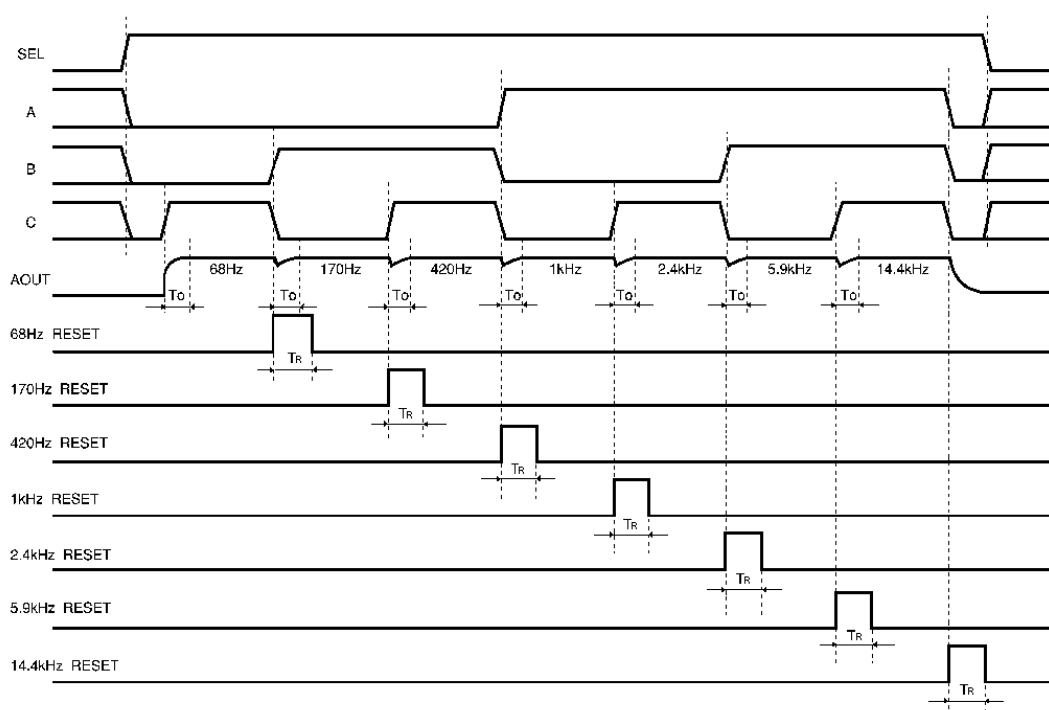


Fig.12

●Cautions on use (BA3835F)

(1) Numbers and data in entries

Numbers and data in entries are representative design values and are not guaranteed values of the items.

(2) Example application circuit

Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.

(3) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

(4) GND potential

Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

(5) Thermal design

Perform thermal design, in which there are adequate margins, by taking into account the power dissipation (Pd) in actual states of use.

(6) Short circuit between terminals and erroneous mounting

Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

(7) Operation in strong electromagnetic field

Using the ICs in a strong electromagnetic field can cause operation malfunction.

(8) Frequency characteristics

The frequency characteristics of this IC are determined by the resistor connected between the R_{REF} terminal and GND. For the specification conditions, the value of this resistor is 100kΩ. If it is necessary to set the frequency characteristics accurately, use a variable resistor

Note: all bands will shift together.

(9) Load characteristics

To convert the bias sense output signal to the GND sense signal, the IC performs a V / I conversion, and then an I / V conversion using a 10kΩ resistor (Typ.) for the output. The AOUT can drive a CMOS load. (e.g. Microprocessor input port) but if it is connected to a circuit with low input impedance, it may cause the output level to drop.

(10) External resistor for the control pin

When using a common port for the output select control and FL drive, you must add a diode and resistor as shown in Fig. 13 to prevent the FL drive "L" voltage from damaging the IC.

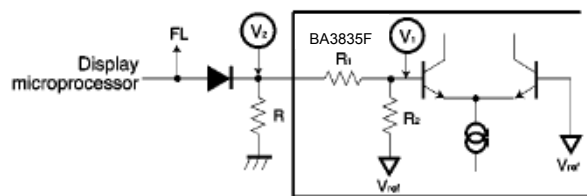


Fig.13

In this case, the "L" voltage applied to the internal comparator input terminal V₁ is given by:

$$V_1 = \frac{R_1 + R}{R_1 + R_2 + R} \times V_{ref}$$

To maintain a noise margin of at least 2.5V with respect to the comparator threshold level V_{REF}, the representative values for V_{REF}, R₁ and R₂ are 1.5V, 20kΩ, and 10kΩ respectively. This gives:

$$\frac{20k\Omega + R}{20k\Omega + 20k\Omega + R} \times 1.5V + 0.25V < 1.5V$$

And from this, the following condition is obtained:

$$R < 30k\Omega$$

In this case, the "L" level voltage V₂ for the IC will be:

$$V_2 < 0.75V$$

(11) Recommended operating ranges

Provided that the IC is operated within the recommended operating conditions and the recommended temperature range, the basic circuit functions are guaranteed. Within these ranges, ratings for electrical characteristics for conditions other than those spec cannot be guaranteed, but the basic function of the band pass filter will be maintained.

(12) Output offset voltage

The relationship between the output offset voltage and the output selection cycle (cycle time) for this IC is shown in Fig. 14. The maximum output offset voltage of 150mV that is given in the electrical characteristics table is under the condition that T_s = 200ms.

When T_s is greater than 50ms, the graph of the output offset voltage is a straight line at 150mV. When T_s is below 50ms, can be sensitive to transient characteristics of the peak hold circuit, the shorter the cycle, the larger the output offset voltage is. Furthermore, the output offset voltage may shift due to soldering or other temperature stresses. Therefore, when setting the spectral analyzer light level, take into consideration the points given above and make sure that the spectral analyzer light does not light up during quiescent periods. Use the chart below as a guide and, if necessary, leave an even a larger margin.

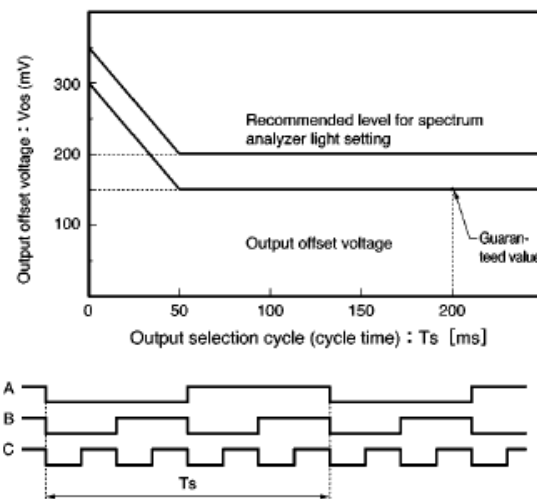


Fig. 14

●Cautions on use (BA3834F)

(1) Numbers and data in entries

Numbers and data in entries are representative design values and are not guaranteed values of the items.

(2) Example application circuit

Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.

(3) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (T_{opr}), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

(4) GND potential

Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

(5) Thermal design

Perform thermal design, in which there are adequate margins, by taking into account the power dissipation (P_d) in actual states of use.

(6) Short circuit between terminals and erroneous mounting

Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

(7) Operation in strong electromagnetic field

Using the ICs in a strong electromagnetic field can cause operation malfunction.

(8) Frequency characteristics

The frequency characteristics of this IC are determined by the resistor connected between the R_{REF} terminal and GND. For the specification conditions, the value of this resistor is 100k Ω . If it is necessary to set the frequency characteristics accurately, use a variable resistor
Note: all bands will shift together.

(9) Load characteristics

To convert the bias sense output signal to the GND sense signal, the IC performs a V/I conversion, and then an I/V conversion using a 10k Ω resistor (Typ.) for the output. The AOUT can drive a CMOS load. (e.g. Microprocessor input port) but if it is connected to a circuit with low input impedance, it may cause the output level to drop.

(10) External resistor for the control pin

When using a common port for the output select control and FL drive, you must add a diode and resistor as shown in Fig. 15 to prevent the FL drive "L" voltage from damaging the IC.

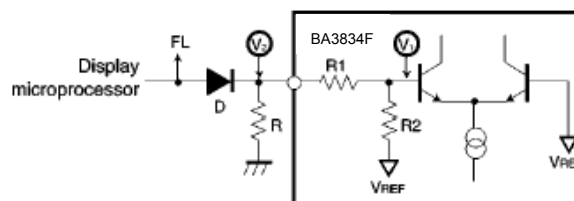


Fig. 15

In this case, the "L" voltage applied to the internal comparator input terminal V_1 is given by:

$$V_1 = \frac{R_1 + R}{R_1 + R_2 + R} \times V_{REF}$$

To maintain a noise margin of at least 2.5V with respect to the comparator threshold level V_{ref} , the representative values for V_{ref} , R_1 and R_2 are 1.5V, 20k Ω , and 10k Ω respectively. This gives :

$$\frac{20k\Omega + R}{20k\Omega + 20k\Omega + R} \times 1.5V + 0.25V < 1.5V$$

And from this, the following condition is obtained : $R < 30k\Omega$

In this case, the "L" level voltage V_2 for the IC will be :

$$V_2 < 0.75V$$

(11) Recommended operating ranges

Provided that the IC is operated within the recommended operating conditions and the recommended temperature range, the basic circuit functions are guaranteed. Within these ranges, ratings for electrical characteristics for conditions other than those spec cannot be guaranteed, but the basic function of the band pass filter will be maintained.

(12) Output offset voltage

The relationship between the output offset voltage and the output selection cycle (cycle time) for this IC is shown in Fig.16. The maximum output offset voltage of 150mV that is given in the electrical characteristics table is under the condition that $T_s = 200ms$.

When T_s is greater than 50ms, the graph of the output offset voltage is a straight line at 150mV. When T_s is below 50ms, can be sensitive to transient characteristics of the peak hold circuit, the shorter the cycle, the larger the output offset voltage is. Furthermore, the output offset voltage may shift due to soldering or other temperature stresses. Therefore, when setting the spectral analyzer light level, take into consideration the points given above and make sure that the spectral analyzer light does not light up during quiescent periods. Use the chart below as a guide and, if necessary, leave an even a larger margin.

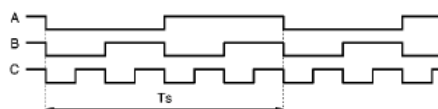
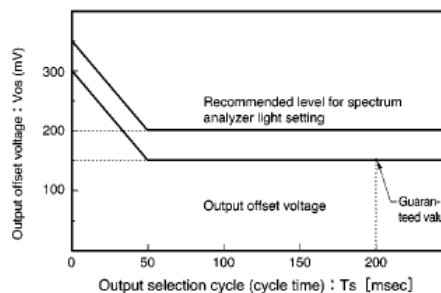
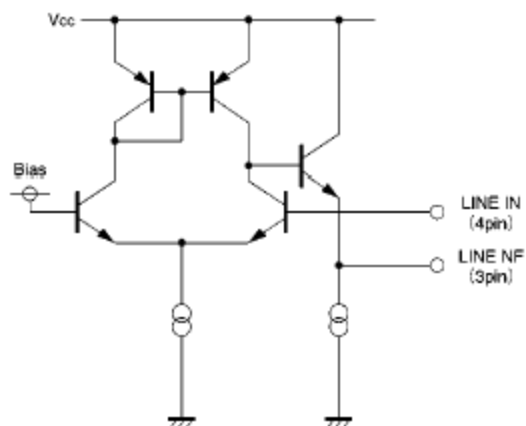


Fig.16

●Circuit operation (BA3830F)

(1) LINE and REC input circuits

The LINE and REC input circuits are configured as differential amplifiers, and the gain can be set to any required value using an external resistor. The input impedance is determined by the external resistor.

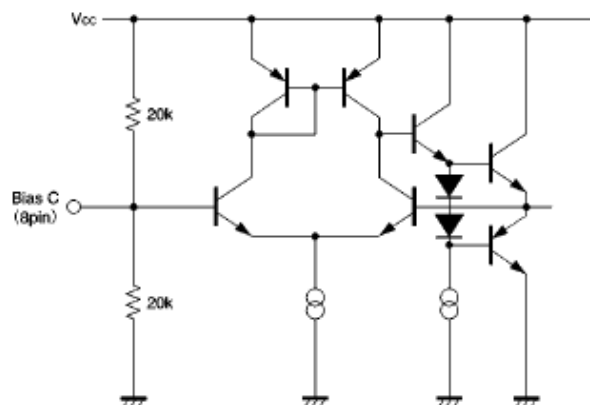


(Note: All resistance values in the internal circuit diagrams noted here are reference values.)

Fig.17

(2) Bias circuit

A bias voltage of $V_{CC}/2$ is applied to each of the circuits. Since the output stage uses a push-pull configuration, a stable bias source can be obtained.



(Note: All resistance values in the internal circuit diagrams noted here are reference values.)

Fig.19

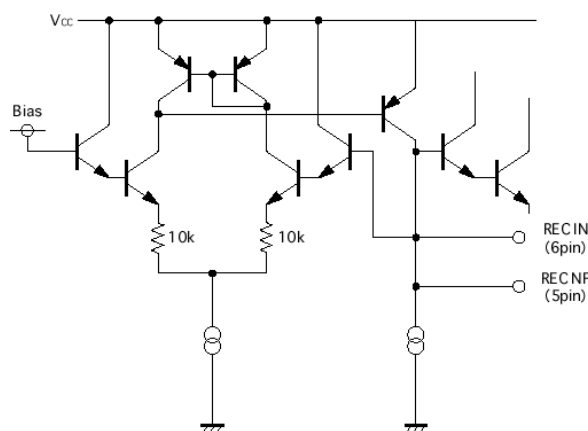


Fig.18

(3) BPF circuit

This is a circuit that selects the required frequency component from the input signal and amplifies it. With this configuration, no external capacitor is needed. In addition, the center frequency is set based on the current, so f_{01} and f_{02} to f_{06} can be set individually, using separate external resistors (pins1 and 2). Q is set to 4.5V (Typ.).

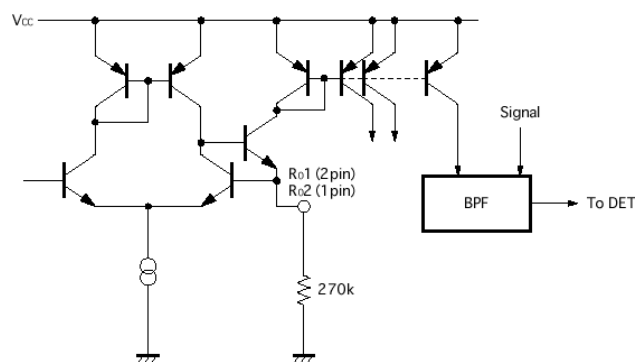


Fig.20

(4) DET circuit

This circuit carries out phase detection on the signal selected and amplified by the BPF, and holds it at the peak level. It is configured so that all of the capacitors are internal. The charge that was charged by the internal capacitors in the DET circuit is set to be discharged at 75ms/V (Typ.), but in order to eliminate any effects of disparity, a reset circuit is also included.

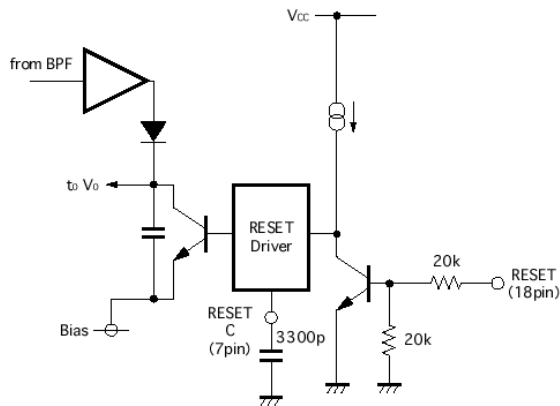


Fig.21

(5) Output section circuit

The signal level held at peak level by the DET undergoes V/ I conversion and is output. Since the next stage supports MOS (high-input impedance), there is a resistance of 33.9kW (44.3kW for REC output only) between the output pin and the GND in the IC, so the output value changes based on the input impedance.

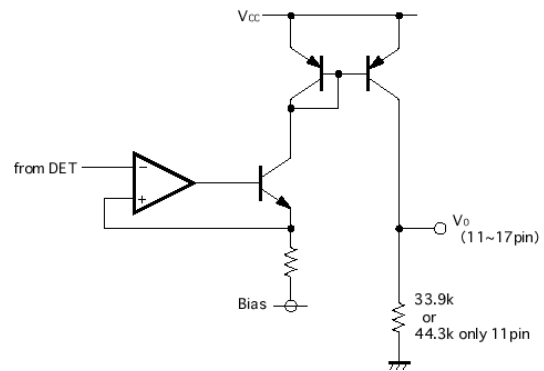
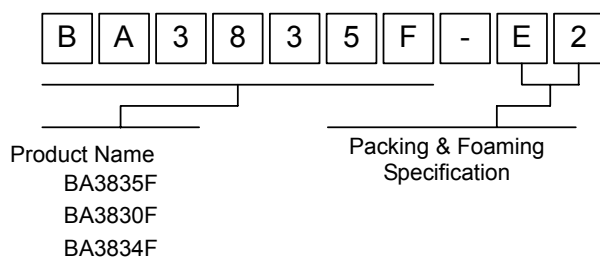
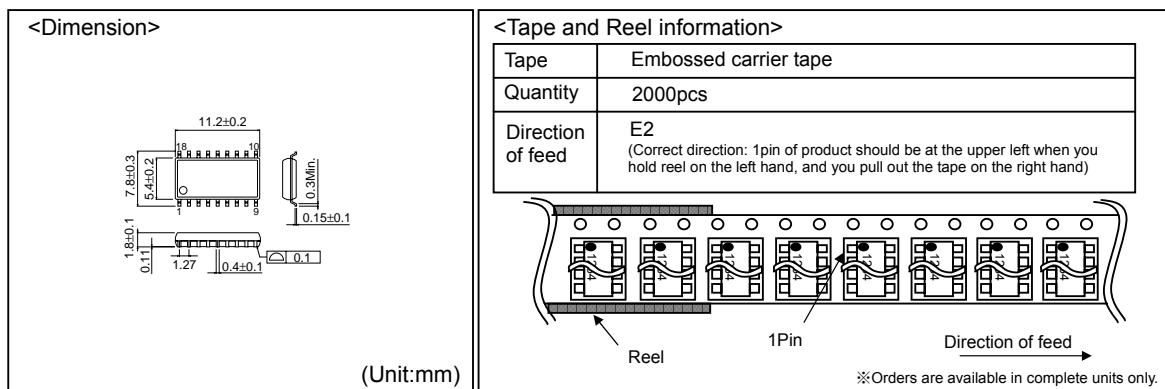


Fig.22

●Order model name selection



SOP18



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