8-BIT 30MSPS
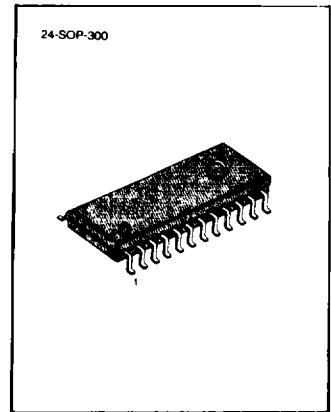## HIGH-SPEED CMOS A/D CONVERTER

The KAD0228 is a CMOS 8-bit A/D converter for video applications.
It is a two-step ping-pong A/D converter consisting of reference
resistor matrix, coarse 4-bit ADC and fine 4-bit ADC. Its maximum
conversion rate is 30MSPS and supply voltage is 5V single.

FEATURES

- **Resolution: 8-bit**
- **Differential Linearity Error: ± 0.6 LSB Typ.**
- **Maximum Conversion Rate: 30MSPS**
- **Sample and Hold Function Included**
- **Low power consumption: Less than 90mW (At 20MSPS Typ.)**
  (Reference Current Excluded)
- **Digital Input: CMOS level**
- **3-state TTL compatible output**
- **Built-in Reference voltage bias circuit**
- **Reference Impedance: 300Ω**
- **Power supply: 5V single**

TYPICAL APPLICATIONS

- PC or computer based video signal processing such as multi-media, frame-grabber, scanner, etc.
- General purpose video applications including camcorder, digital video (TV/VCR), broadcasting and studio equipments.
- Medical electronics such as ultra-sound, imaging.
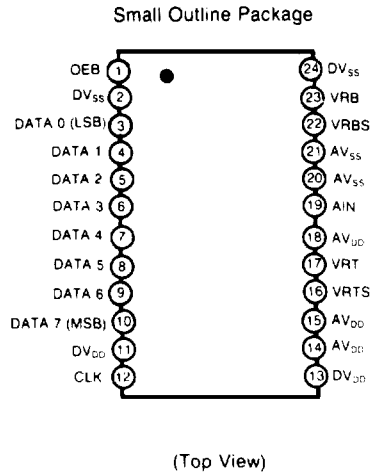- High speed instrumentations such as digital scope, transit recorder, radar.

24-SOP-300

3

ORDERING INFORMATION

Device	Package	Temperature Range
KAD0228ED	24 SOP	0 ~ + 70°C

BLOCK DIAGRAM

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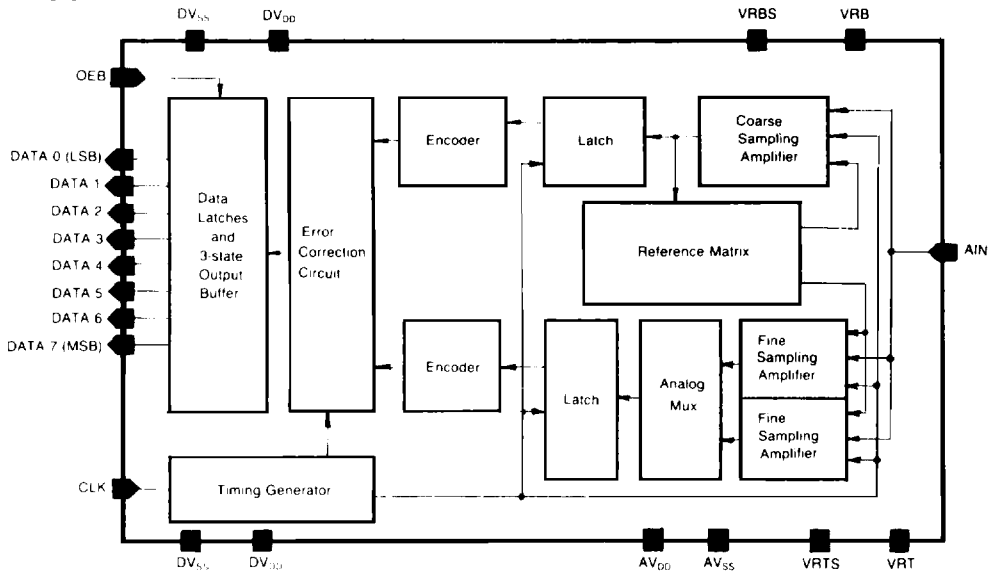
PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OEB	I	3-state output enable. 3-state when OEB = V_{DD}, enable when OEB = V_{SS}
2	DV_{SS}	–	Digital ground for digital output buffer
3	DATA 0	O	Digital output data (LSB)
4	DATA 1	O	Digital output data
5	DATA 2	O	Digital output data
6	DATA 3	O	Digital output data
7	DATA 4	O	Digital output data
8	DATA 5	O	Digital output data
9	DATA 6	O	Digital output data
10	DATA 7	O	Digital output data (MSB)
11	DV_{DD}	–	Digital supply for digital output buffer
12	CLK	I	CMOS digital clock input
13	DV_{DD}	–	Digital supply for digital interior circuitry
14	AV_{DD}	–	Analog supply for comparator, reference resistor switch
15	AV_{DD}	–	Same as pin No. 14
16	VRTS	O	Internal self-biased reference top. Shorted with VRT pin (17), generates 2.6 volts.
17	VRT	I	Reference resistor top side
18	AV_{DD}	–	Same as pin No. 14
19	AIN	I	Analog input
20	AV_{SS}	–	Analog ground for comparator, reference resistor switch
21	AV_{SS}	–	Same as pin No. 20
22	VRBS	O	Internal self-biased reference bottom. Shorted with VRB pin (23), generates 0.6 volts.
23	VRB	I	Reference resistor bottom side
24	DV_{SS}	–	Digital ground for digital interior circuitry

PIN CONFIGURATION
(24 SOP)

Small Outline Package

```
         OEB  (1)    ●      (24) DVss
         DVss (2)            (23) VRB
  DATA 0 (LSB)(3)            (22) VRBS
       DATA 1 (4)            (21) AVss
       DATA 2 (5)            (20) AVss
       DATA 3 (6)            (19) AIN
       DATA 4 (7)            (18) AVDD
       DATA 5 (8)            (17) VRT
       DATA 6 (9)            (16) VRTS
  DATA 7 (MSB)(10)           (15) AVDD
         DVDD (11)           (14) AVDD
         CLK  (12)           (13) DVDD
```

(Top View)

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristics	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Analog Input Voltage	AIN	V_{SS} to V_{DD}	V
Reference Input Voltage	VRT, VRB	V_{SS} to V_{DD}	V
Storage Temperature Range	T_{stg}	-55 to $+125$	°C
Operating Temperature Range	T_{opr}	-20 to $+75$	°C
ESD Susceptibility (Note 3)	V_{esd}	$> \pm 1500$	V

Note 1: ABSOLUTE MAXIMUM RATINGS are those values beyond which the device may be damaged permanently.
　　　　Normal operation is not guaranteed at or above these extremes.
Note 2: All voltages are measured with respect to the V_{SS} voltage level otherwise specified.
Note 3: 100pF discharged through a 1.5kΩ resistor (Human body model).

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RECOMMENDED OPERATING CONDITIONS (Note 4)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	$AV_{DD} - AV_{SS}$ $DV_{DD} - DV_{SS}$	4.75	5.0	5.25	V
Supply Voltage Difference	$AV_{DD} - DV_{DD}$	-0.1	0.0	0.1	V
Reference Input Voltage (Note 5)	VRB VRT	0 —	0.6 2.6	— 2.8	V
Analog Input Voltage	AIN	VRB	—	VRT	V
Clock High Time Clock Low Time	t_{pwH} t_{pwL}	15 15	— —	— —	ns
Digital Input "L" Voltage Digital Input "H" Voltage	V_{IL} V_{IH}	— 4.0	— —	1.0 —	V
Operating Temperature	T_{opr}	0	—	70	°C

Note 4. It is strongly recommended that all the supply pins (AV_{DD}, DV_{DD}) be powered from the same source.
Note 5. The value of (VRB - VRT) can be moved to the up side (2 ~ 4V), but characteristics can't be guaranteed.

STATIC ELECTRICAL CHARACTERISTICS

(Converter Specifications: $AV_{DD} = DV_{DD} = 5V$, $AV_{SS} = DV_{SS} = 0V$, Ta = 25°C, VRB = 0.6V, and VRT = 2.6V unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Current	IREF	VRT = 2.6V, VRB = 0.6V	5.0	6.7	10	mA
Reference Resistance	RREF		200	300	400	Ω
Internal Bias	VRBS VREF	Short VRT and VRTS Short VRB and VRBS	0.55 1.9	0.60 2.0	0.65 2.1	V
Digital Input Low Current	IIL	$V_{DD} = 5.25$, VIL = V_{SS}	—	—	1	μA
Digital Input High Current	IIH	$V_{DD} = 5.25$, VIH = V_{DD}	—	—	1	μA
Digital Output Current (Output Enable)	IOL IOH	$V_{DD} = 4.75$, VOL = 0.4V VOH = $V_{DD} - 0.5V$ OEB = VSS	3.5 -1.1	— —	— —	mA
Digital Output Current (Output High Imp.)	IOZL IOZH	$V_{DD} = 5.25$, VOL = VSS VOH = V_{DD} OEB = V_{DD}	— —	— —	16 16	uA
Offset Voltage Error	EOT EOB	$V_{DD} = 5.0$, VRT = 2.6V, VRB = 0.6V	0 0	-25 $+20$	-68 $+40$	mV
Differential Linearity Error Integral Linearity Error	ELD ELI	$V_{DD} = 5.0$, VRT = 2.6V, VRB = 0.6V	—	± 0.6 ± 0.8	± 1.0 ± 1.2	LSB

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DYNAMIC CHARACTERISTICS

(Converter Specifications: $AV_{DD} = DV_{DD} = 5V$, $AV_{SS} = DV_{SS} = 0V$, $Ta = 25°C$, $VRB = 0.6V$, and $VRT = 2.6V$ unless otherwise specified.)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Conversion Rate	f_C	AIN = 0.6V to 2.6V, 1MHz sine wave	30	—	—	MSPS
Dynamic Supply Current	I_{VDD}	$F_S = 20MHz$, AIN = NTSC ramp input	—	18	27	mA
Digital Output Data Delay (Note 6)	t_d	$OEB = V_{SS}$	—	18	30	ns
Digital Output Data Delay (Output High Imp.)(Note 7)	t_{disH}		—	—	100	ns
	t_{disL}		—	—	100	
Digital Data Valid Time (Note 7)	t_{eneH}		—	—	100	ns
	t_{eneL}		—	—	100	
Signal-to-Noise Ratio	SNR1	CK = 20MHz, AIN = 1MHz sine wave	—	45	—	dB
	SNR2	2MHz sine wave	—	45	—	dB
	SNR3	4MHz sine wave	—	41	—	dB
Differential Phase	DP	NTSC 20 IRE mod Ramp signal, $F_s = 14.3MSPS$	—	0.7	—	deg
Differential Gain	DG		—	1.0	—	%
Sampling Time Offset	t_{sto}			5	10	ns

Note 6:See "Delay Timing Diagram"

Note 7:See "3-State Putput Test Circuit and Timing diagram"

DELAY TIMING DIAGRAM

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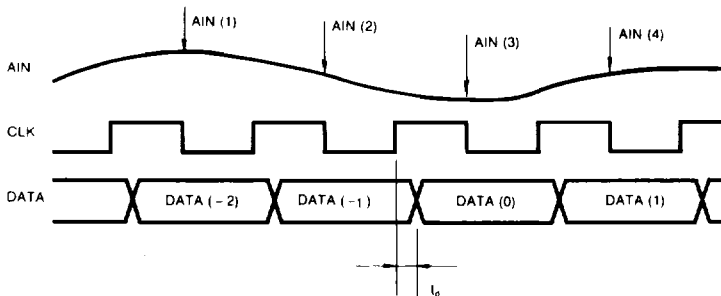
I/O CHART

Index	Analog Input (V)	Digital Output	
0	~ 0.6078125	00000000	
1	0.6078125 ~ 0.6156250	00000001	VRB = 0.6V
2	0.6156250 ~ 0.6234375	00000010	VRT = 2.6V
.....	.....	.....	
126	1.5921875 ~ 1.6000000	01111111	1LSB = 7.8125mV
127	1.6000000 ~ 1.6078125	10000000	
128	1.6078125 ~ 1.6156250	10000001	
.....	.....	.....	
254	2.5843750 ~ 2.5921875	11111110	
255	2.5921875 ~	11111111	

3-STATE OUTPUT TEST CIRCUIT AND TIMING DIAGRAM
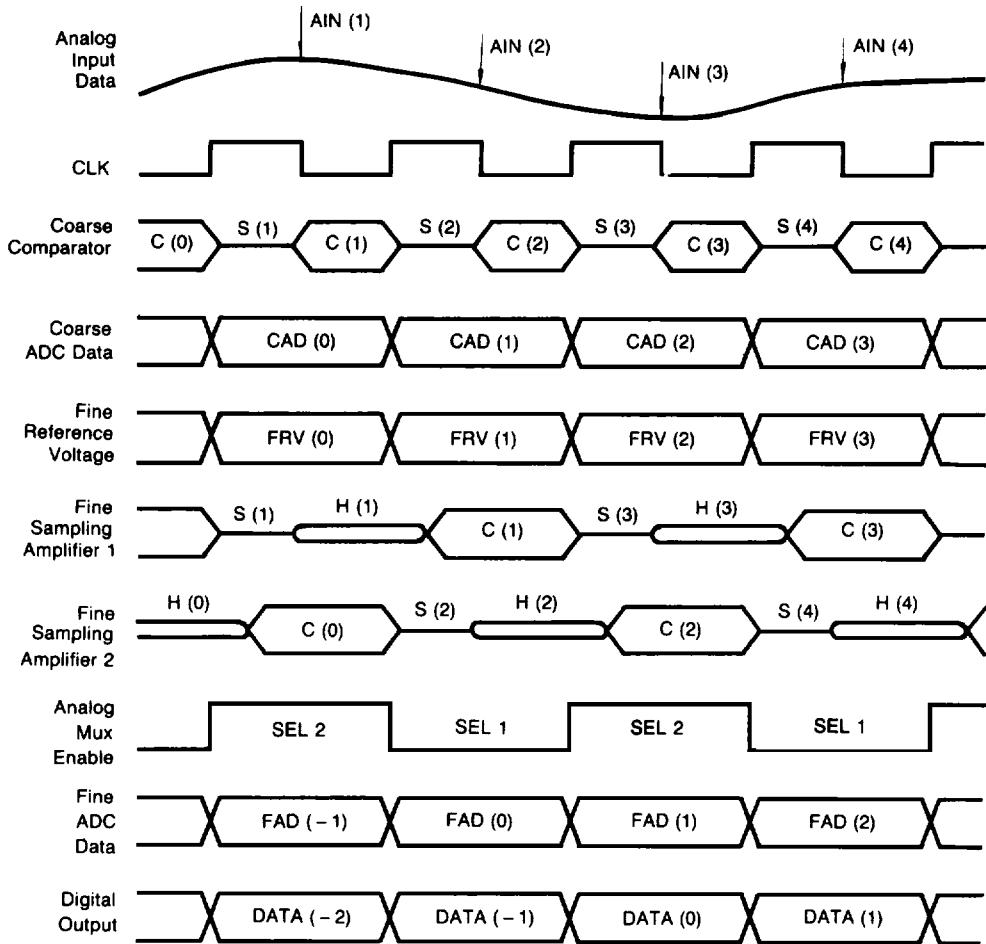
SAMSUNG ELECTRONICS
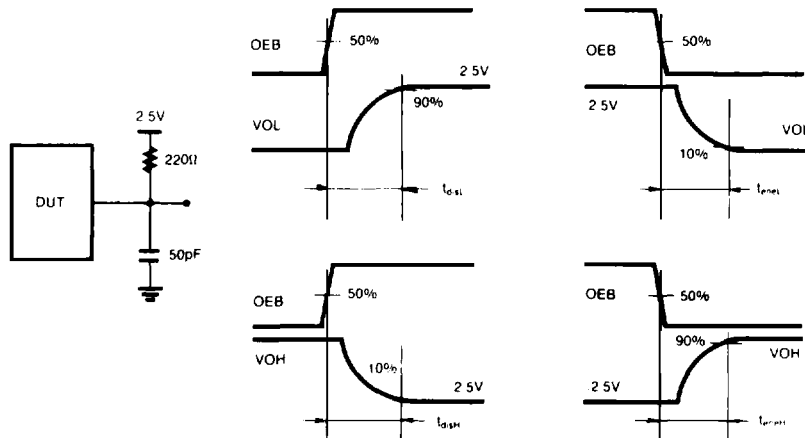
FUNCTIONAL DESCRIPTION

1. KAD0228 is a two-step ping-pong A/D converter comprising 4-bit coarse ADC and fine ADC of 4.459 bit, approximately. Coarse ADC is composed of 15 auto zero comparators, and fine ADC has 22 sampling amplifier pairs of which the two sampling amplifier operate alternately in a ping-pong manner, and also has 22 analog MUXs and 22 latching comparators.

2. Using a CMOS auto zero comparator and switching 1 ot 16 different sets of reference voltage to the fine sampling amplifier bank according to the coarse ADC state, the difficulties in implementing high accuracy (more than 8 bit) DAC was eliminated, thus low-power, high-performance, high-speed ADC was achieved. KAD0228 uses an averaging method to reduce the charge injection mismatch in the sampling switches, so the overall differential non-linearity error is enhanced.

3. KAD0228 operates as follows (See Timing Diagram):
   During the first "H" cycle of external clock the analog input data is sampled and tracked, and the input is held from the falling edge of the CLK (the analog input is abbreviated to AIN in the timing diagram), which is compared with the 16-level coarse reference voltage and latched to result in data CAD. According to the coarse ADC data, the fine reference voltage FRV is set and fed to the fine sampling amplifier bank. This FRV voltage set is compared with the sampled analog input, and resulted in the fine sampling amplifier data. The fine sampling amplifier operates in a ping-pong style to reproduce the analog data with sufficiently large gain, and then MUXed to the latching comparators. Latching comparator bank generates the fine ADC data (FAD), which is used to generate the digital output (DATA) together with the CAD data. The overall pipeline delay is 2.5 clock.

4. KAD0228 has the correction scheme of the error which comes from the mismatch in the coarse ADC and the fine sampling amplifier offset. This error correction scheme can handle up to 3 LSBs, and hence helps enhance the differential linearity.

5. Inside KAD0228, reference resistors are placed between AV_{DD} and VRTS, and between AV_{SS} and VRBS so that VRTS and VRBS generate the 2.6V, and 0.6 Volt reference respectively. In order to utilize the internal self-biased reference voltage, the VRTS pin (16) is to be shorted with VRT pin (17) and the VRBS pin (22) is to be shorted with the VRB pin (23). It is not recommended to take advantage of the self-biased internal reference voltage in case of applying KAD0228 in a special system which offers high accuracy, though (See Reference Circuit Diagram).
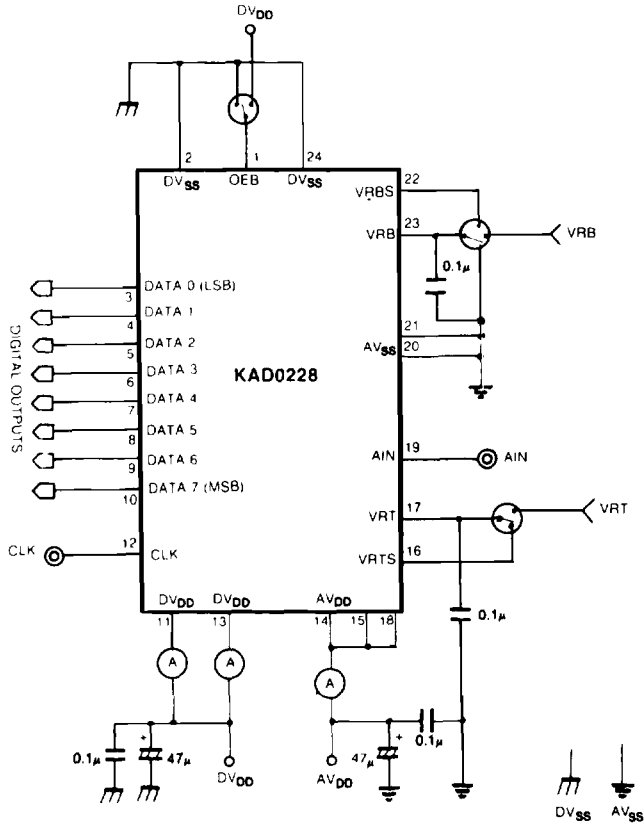
REFERENCE CIRCUIT DIAGRAM

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TIMING DIAGRAM

| Analog Input Data | AIN (1) | AIN (2) | AIN (3) | AIN (4) |

CLK

Coarse Comparator: C (0) S (1) C (1) S (2) C (2) S (3) C (3) S (4) C (4)

Coarse ADC Data: CAD (0) CAD (1) CAD (2) CAD (3)

Fine Reference Voltage: FRV (0) FRV (1) FRV (2) FRV (3)

Fine Sampling Amplifier 1: S (1) H (1) C (1) S (3) H (3) C (3)

Fine Sampling Amplifier 2: H (0) C (0) S (2) H (2) C (2) S (4) H (4)

Analog Mux Enable: SEL 2 SEL 1 SEL 2 SEL 1

Fine ADC Data: FAD (– 1) FAD (0) FAD (1) FAD (2)

Digital Output: DATA (– 2) DATA (– 1) DATA (0) DATA (1)
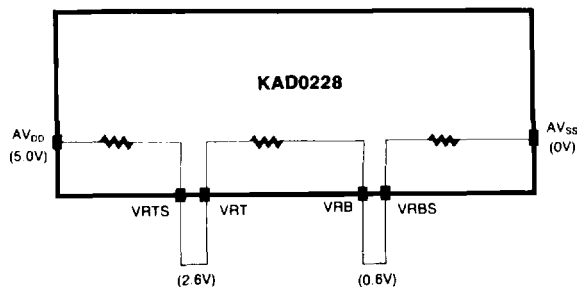
TEST CIRCUIT (Note 8)

Note 8: AV_{DD} and DV_{DD} are needed to be out from common source.

Make the distance between CLK source and CLK DUT pin as short as possible.

Test circuit can be changed because of test equipment and test items.

A/D Input Amplifier and Clamping Circuit