

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

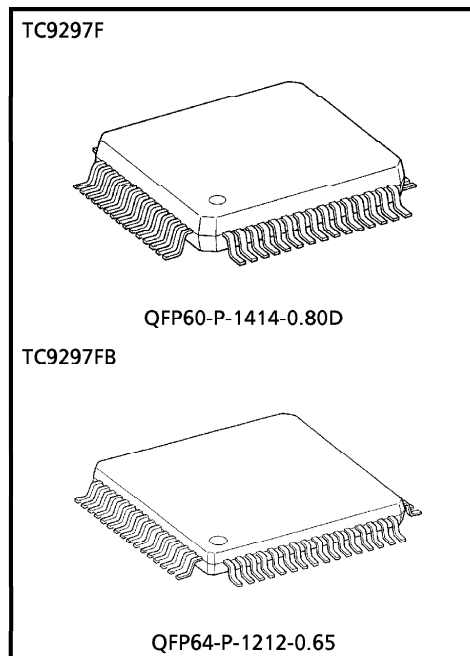
TC9297F, TC9297FB

LCD DRIVER WITH ON-CHIP KEY INPUT

TC9297F/FB are an LCD driver IC with on-chip key input, which is serial data controlled.

FEATURES

- Supports switching between 1/2 and 1/3 duty, and between 1/2 and 1/3 bias.
- Displays up to 80 segments in 1/2-duty mode and up to 117 segments in 1/3-duty mode.
- All display segments can be either off or on. Outputs of pins S₃₆-S₃₉ can be switched between segment output and LED driver output.
- Supports key input from up to 30 keys.
- 3-wire configuration for controller connection.



Weight

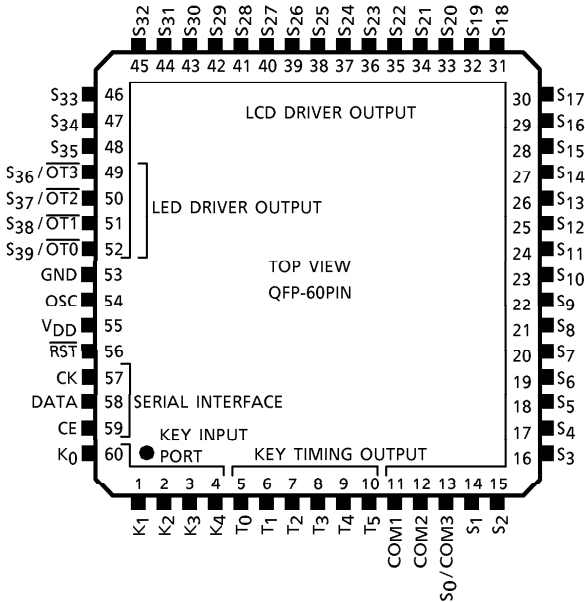
QFP60-P-1414-0.80D : 1.10g (Typ.)
QFP64-P-1212-0.65 : 0.45g (Typ.)

961001EBA1

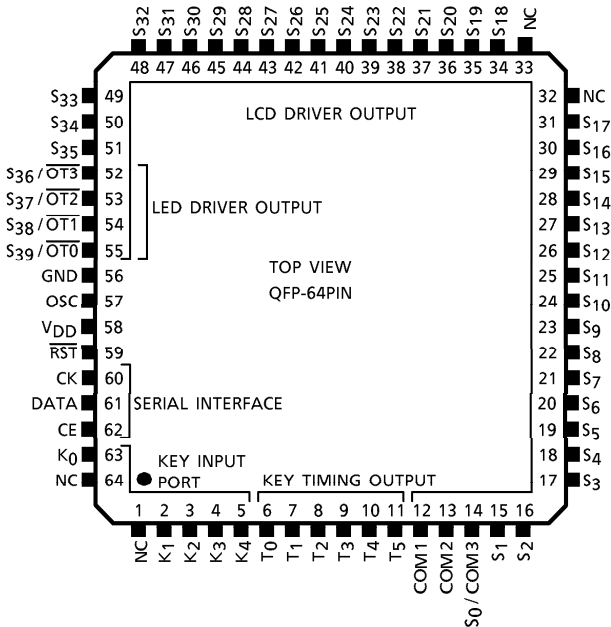
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN CONNECTION

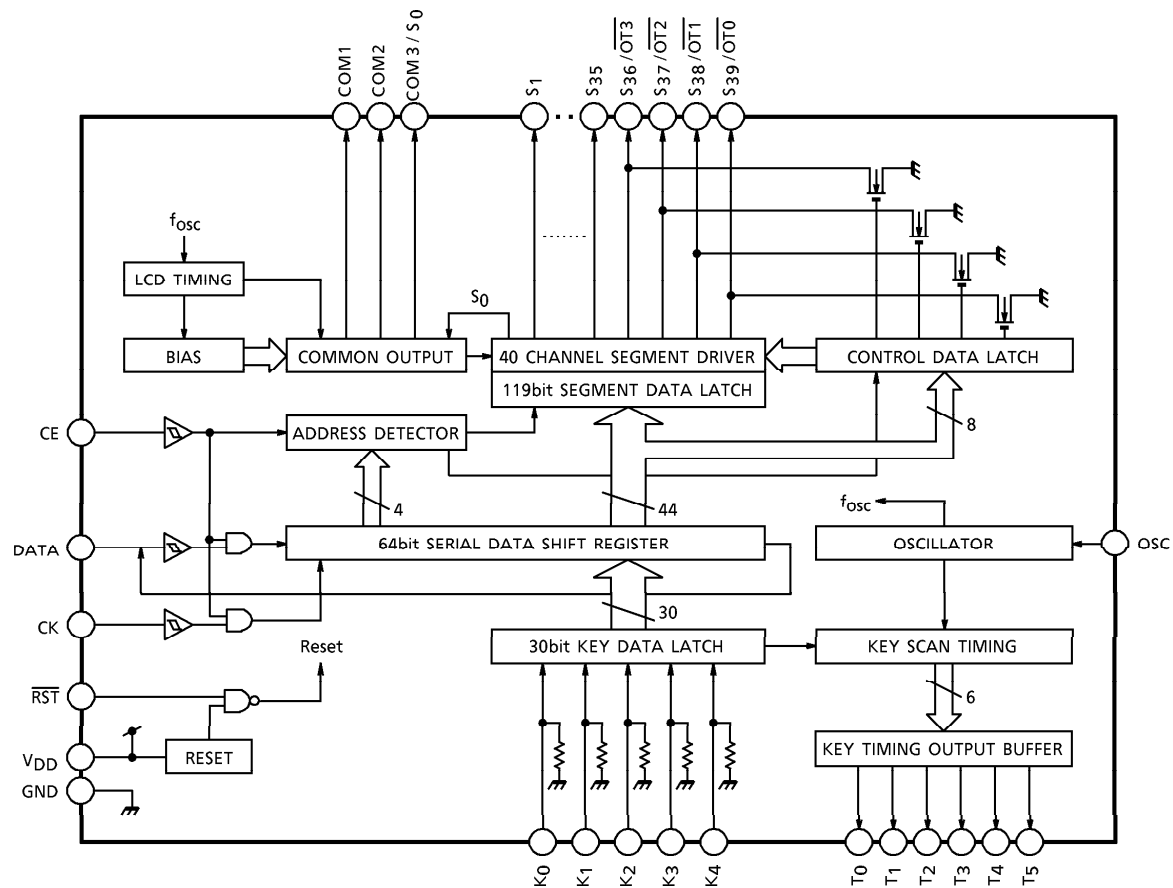
(TC9297F)



(TC9297FB)

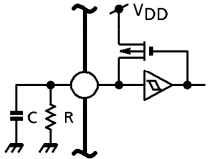
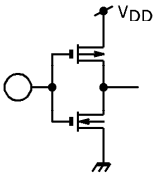
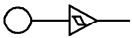
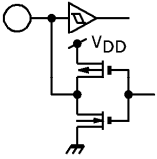
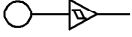


BLOCK DIAGRAM



PIN FUNCTIONS (Data in parentheses are for TC9297FB)

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
55 (58)	V _{DD}	Power supply input pin	Power supply input pin. Normally supplied with VRST-5.5V. Power-on reset function resets system when powered up and when V _{DD} drops below 3V (Typ.).	—
53 (56)	GND	Ground pin		
60 (63) 1 (2) ⋮ 4 (5)	K ₀ K ₁ ⋮ K ₄	Key-scan input pin	Key-scan input pins. Data from up to 6 × 5 = 30 keys can be input by a key matrix with key scan output pins T ₀ -T ₅ . When high is input to pins, key scan begins. These are I/O pins with built-in pull-down resistors.	
5 (6) ⋮ 10 (11)	T ₀ ⋮ T ₅	Key scan timing output pin	Key scan timing output pins. Due to key matrix configured using load resistor R _{ON} on the N-channel, no diodes are required. Output is normally high. When high is input to key scan input pins K ₀ -K ₄ , key scan begins.	
11 (12) 12 (13)	COM1 COM2	LCD common output pin	LCD segment output/common output pins. When set to 1/2-duty, can display up to 80 segments in a matrix of pins COM1, 2 and S ₀ -S ₃₉ ; when set to 1/3-duty, up to 117 segments in a matrix of COM1-3 and S ₁ -S ₃₉ . In 1/3-duty mode, pin S ₀ is used as COM3.	
13 (14)	S ₀ / COM3	LCD segment output /common output pin		
14 (15~31) ⋮ 48 (34~51)	S ₁ ⋮ S ₃₅	LCD segment output pin	LCD segment output / LED driver output pins. When set to 1/2-duty, can display up to 80 segments in a matrix of pins COM1, 2 and S ₀ -S ₃₉ ; when set to 1/3-duty, up to 117 segments in a matrix of COM1-3 and S ₁ -S ₃₉ .	
49 (52) ⋮ 52 (55)	S ₃₆ / OT3 ⋮ S ₃₉ / OT0	LCD segment output / LED driver output pin	Pins S ₃₆ -S ₃₉ also serve as LED driver pins. The LED driver output becomes N-ch open driver output, and large-current drive allows direct LED display.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
54 (57)	OSC	Crystal oscillator output pin	Oscillates when connected to an external crystal. The oscillation frequency is expressed by the frequency expression : $f_{OSC} \approx 1.5 / (C \cdot R)$ [Hz] For instance, when $C = 0.01 \mu F$, $R = 30 k\Omega$: $f_{OSC} \approx 5 kHz$	
56 (59)	\overline{RST}	System reset input pin	System reset input pin. While RST input is low, the oscillator stops, all internal data are reset, and the LCD output and key scan output pins are fixed to high. There is a built-in power-on reset circuit, so this pin should normally be connected to V_{DD} .	
57 (60)	CK	Clock input pin	Serial interface pins that send to and receive from the controller display data and key input data, and the data to control these. Data send / receive is not performed while pin CE is low, but when CE goes high, begins at the DATA pins in sync with the clock input of the CK input pin. All these pins have built-in Schmitt input circuits.	
58 (61)	DATA	Data I/O pin		
59 (62)	CE	Chip enable input pin		

○ CONTENT OF ADDRESS DATA

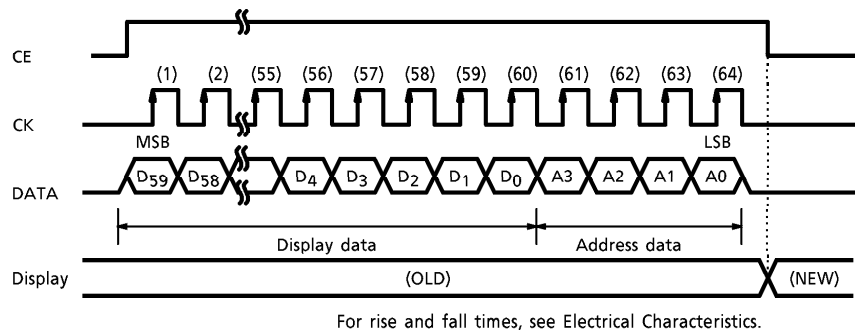
DUTY	A3	A2	A1	A0	ADDRESS (HEX)	D0	D1	D2	D3	D4	D5	D6	D7	D8~D32	D33~D39	D40~D59					
1/2	0	*	1	1	1, 3, 5, 7	S0~S19 Display Data										—					
						S0		S1		S2		S3		S4~S19							
						COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2 System	COM1 System	COM2, 1 System							
	0	*	1	*	2, 3, 6, 7	S20~S39 Display Data										—					
COM2 System	COM1 System	COM2 System	COM1 System	S21	COM2 System	COM1 System	COM2 System	COM1 System	S22	COM2 System	COM1 System	S23	COM2 System	COM1 System	S24~S39						
																	COM2, 1 System				
1/3	0	*	1	1	1, 3, 5, 7	S0~S19 Display Data										COM3, 2, 1 System					
						S0		S1		S2~S19											
						—		COM3 System		COM2 System		COM1 System		COM3, 2, 1 System							
	0	*	1	*	2, 3, 6, 7	S20~S39 Display Data										COM3, 2, 1 System					
S20						S21		S22		S23		S22~S39									
*	1	0	0	0	8	COM3 System	COM2 System	COM1 System	COM3 System	COM2 System	COM1 System	LCD CONTROL	COM3, 2, 1 System	"0"	—						
																SET SEGMENT OUTPUT /LED DRIVER	S37 /OT2	S36 /OT3	Duty	Bias	"0"
	LED DRIVER CONTROL										DISPLAY CONTROL		—								
1	0	0	1	9	OT0	OT1	OT2	OT3	OT3	OP	BL	LT		"0"	—						
													KEY DATA (OUTPUT)								
1	0	1	0	A	KON	KWK	K01	K02	K03	K04	K05	K06	K07~K30	"0"							

* : Don't care
— : Invalid data

OPERATING INSTRUCTIONS

1. Input format for display data and mode data

- Display data input timing is as shown below (when set to 1/3-duty) :



For rise and fall times, see Electrical Characteristics.

- The last 4 bits of data are the address data.
- For segment data and control data corresponding to the segment data output being used, set all bits used.
- Segment data corresponding to the unused segment outputs of the MSB may be omitted.
- Segment data may be set to either address 1H or 2H.
- Do not set segment data until the data at address 8H have been set. Otherwise, it may be impossible to set segment data correctly.
- Data input is synchronized with the clock rising edge.

(1) 1/2-duty (80-segment) data format

The format for display data in 1/2-duty mode is as shown below:

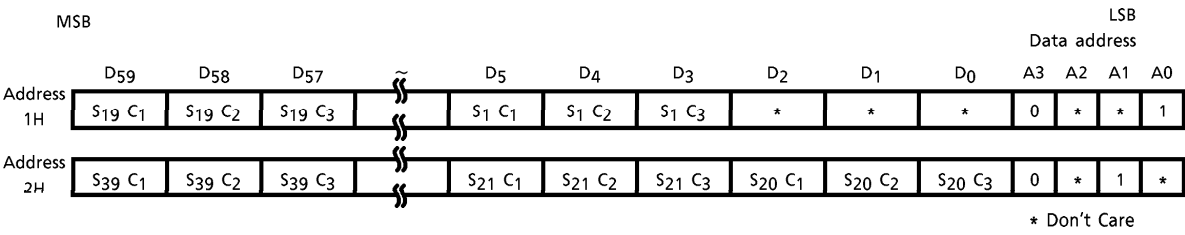
MSB												LSB			
												Data address			
Address	D39	D38	D37	D36	D35	D34	~	D3	D2	D1	D0	A3	A2	A1	A0
1H	S19 C1	S19 C2	S18 C1	S18 C2	S17 C1	S17 C2	~	S1 C1	S1 C2	S0 C1	S0 C2	0	*	*	1
2H	S39 C1	S39 C2	S38 C1	S38 C2	S37 C1	S37 C2	~	S21 C1	S21 C2	S20 C1	S20 C2	0	*	1	*

* Don't Care

- In this case, segment data controlled by COM3 are invalid, and data need not be set.
- Pins S0-S39 can be used for segment output.

(2) 1/3-duty (80-segment) data format

The format for display data in 1/3-duty mode is as shown below:



- In this case, the pin is used as COM3, but set data as for the S₀ pin.
(Note that the set data are non-functional.)
- Pins S₁-S₃₉ can be used for segment output.

These data bits control on/off switching of the display corresponding to the common outputs. A waveform corresponding to display on/off is output to the segment output corresponding to common/segment data. Set "1" for display on and "0" for off. To set data for pins S₀-S₁₉ and S₂₀-S₃₉ independently, specify the address to 1H and 2H respectively.

When data for pins S₀-S₁₉ and S₂₀-S₃₉ overlap, identical data can be transferred simultaneously with a single serial data transfer by specifying 3H as the address. When there are unused segments of the MSB, the data setting for unused segments of the MSB omit and it can possible to set from used segment data of the MSB.

(Example) When up to 24 segments are used in 1/3-duty mode.



(3) Duty and bias bits

	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
Address 8H	0	0	Bias	Duty					1	0	0	0
			BIAS	DUTY								
*			0	0								
			0	1								
			1	0								
			1	1								

* (Note) These data are reset to "0" at reset.

(4) BL and LT bits

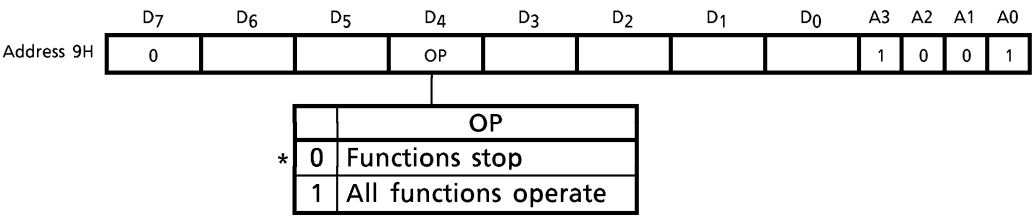
	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
Address 9H	0	LT	BL						1	0	0	1
		LT	BL									
*		0										
		1										
		0										
		1										

Even when the display is set to all on or all off, the display data prior to setting is retained and no resetting of display data is required.
It is also possible to set new data while all on or all off.

* (Note) These data are reset to "0" at reset.

** (Note) When both BL and LT are "1", BL takes priority.

(5) OP bit



The OP bit controls the operating and stopping of the LCD driver, key scan and other functions. When it is reset to "0", all operations stop, the LCD driver output and key scan output pins are fixed to high, and the oscillator stops.

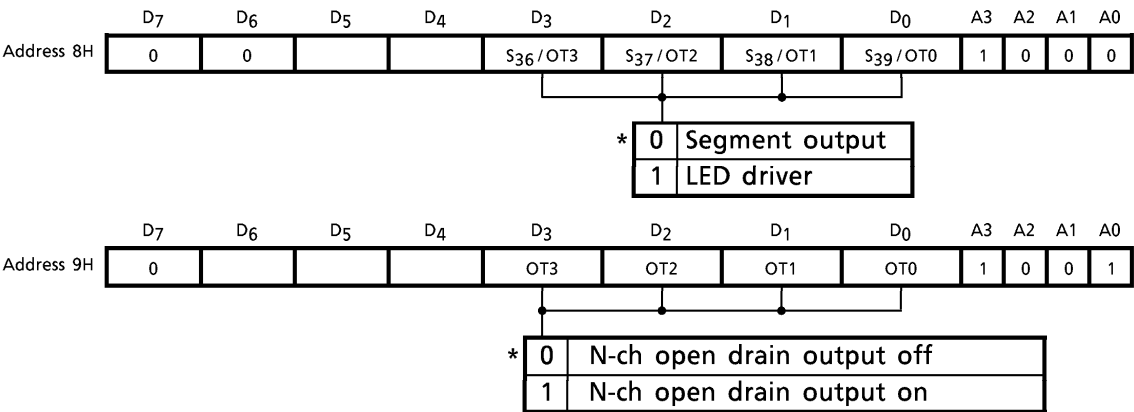
The data of control bits prior to setting is retained, and new data can be set.

When this pin is set to "1", the oscillator, LCD driver and key scan operate.

At reset, this bit is reset to "0". Initialize control data and display data in this state.

* (Note) These data are reset to "0" at reset.

(6) Segment output/LED driver switching bits and LED driver control bits



The segment output/LED driver switching bits switch between segment output and the LED driver output. Resetting these bits to "0" selects segment output; setting to "1" selects LED driver output. When set to segment output, display data are output and the LCD display is turned on and off; when set to LED driver output, output is turned on and off by the LED driver control bit.

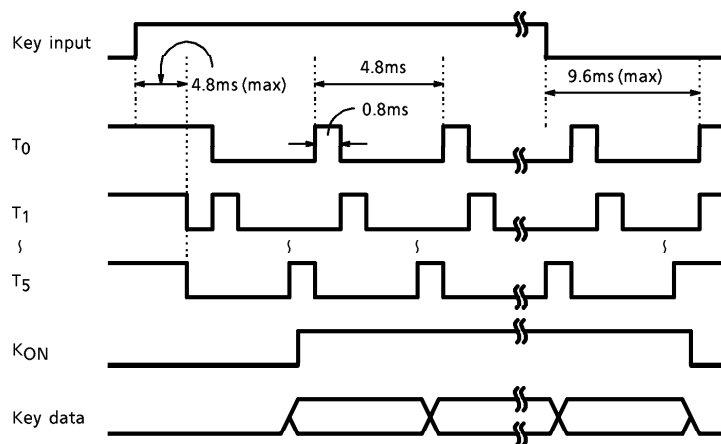
The LED driver is of N-ch open-drain structure. Setting the LED driver control bit to "0" turns off N-ch open output; setting to "1" turns off N-ch open output.

When set to segment output, the corresponding LED driver control data are invalid; conversely, when set to LED driver, the corresponding segment output display data are invalid.

When S36-S39 are used for LED driver output, data must not be set to address 9H until the segment/LED switching bit of the corresponding address 8H has been set to "1".

* (Note) These data are reset to "0" at reset.

(3) Key scan timing is as shown below:



(Note) When f_{osc} is 5kHz.

When high is input to the key input pin, key scanning begins within not more than one cycle (4.8ms when f_{osc} is 5kHz), and the key data corresponding to the key timing is input. After one more cycle of key scanning, K_{ON} is set to "1" and key data are entered and upgraded every cycle. When the key is released, key scanning stops within not more than two cycles (9.6ms when f_{osc} is 5kHz), and all key data are reset to "0".

Thus, key data must be accessed during key scanning.

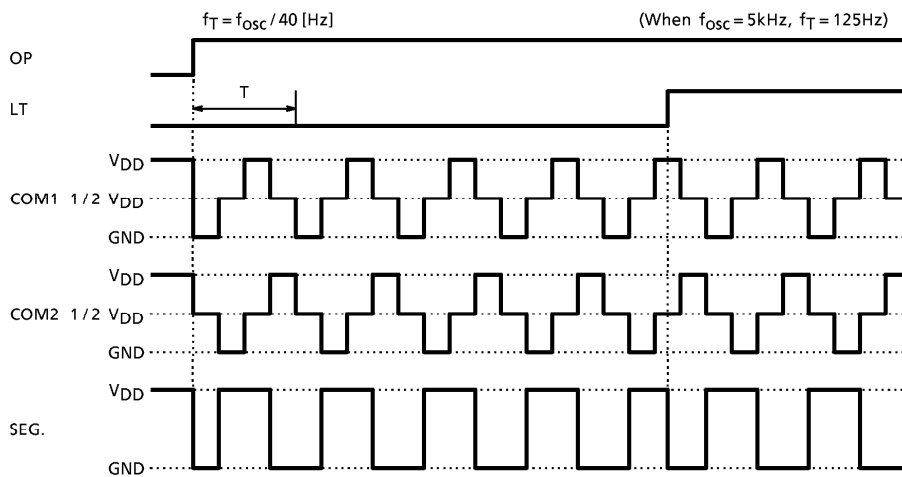
To access key data, pin CE may be held low after input of address data.

The result is standby until key input occurs. In this state, the K_{ON} bit is output to the data pin as-is, so that it is "1" when there is key input and "0" when there is not.

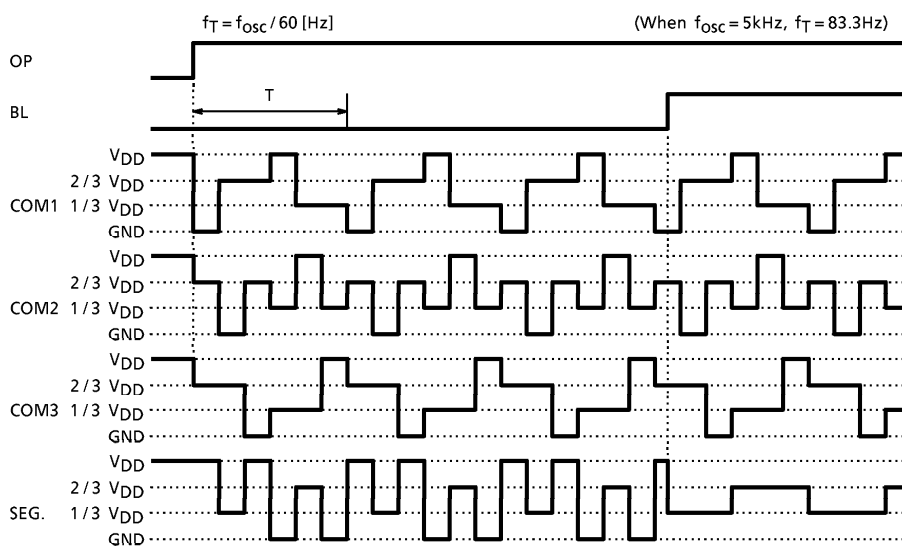
If key data are continuously accessed based on the state of K_{ON} , key data can be effectively fetched.

3. The output waveforms of the LCD driver are as shown below.

- 1/2 duty, 1/2 bias (COM1 system off, COM2 system on)



- 1/3 duty, 1/3 bias (COM1 system on, COM2 system off, COM3 system on)



MAXIMUM RATINGS (Ta = 25°C)

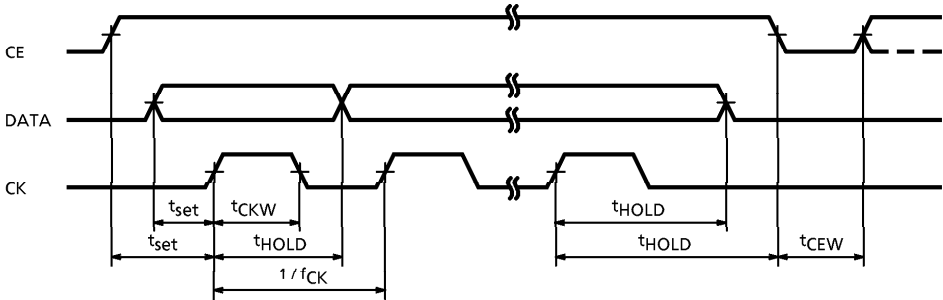
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	- 0.3~7.0	V
Input Voltage	V _{IN}	- 0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	- 40~85	°C
Storage Temperature	T _{stg}	- 65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 4.5~5.5V, Ta = - 40~85°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V _{DD}	—	—	V _{RST}	5.0	5.5	V
Power On Reset Voltage		V _{RST}	—	—	2.5	3.0	3.5	V
Operating Supply Current		I _{DD1}	—	V _{DD} = 5V, f _{osc} = 5kHz, No load	—	0.4	1.0	mA
Stand-by Current		I _{DD2}	—	OP = “0”, V _{DD} = 5V	—	120	250	μA
Input Voltage	“H” Level	V _{IH}	—	K ₀ ~K ₃ , CE, DATA, CK, $\overline{\text{RST}}$	V _{DD} × 0.8	~	V _{DD}	V
	“L” Level	V _{IL}	—	K ₀ ~K ₃ , CE, DATA, CK, $\overline{\text{RST}}$	0	~	V _{DD} × 0.2	V
SCHMITT Voltage Width		V _{SCH}	—	V _{DD} = 5V, CE, DATA, CK	—	1.0	—	V
Input Leak Current	“H” Level	I _{IH}	—	V _{IN} = V _{DD} , CE, DATA, CK, $\overline{\text{RST}}$	—	~	± 1.0	μA
	“L” Level	I _{IL}	—	V _{IN} = 0V, CE, DATA, CK, $\overline{\text{RST}}$	—	~	± 1.0	μA
Output Voltage	1 / 2 Level	V _{1 / 2}	—	V _{DD} = 5V COM1, COM2	1 / 2V _{DD} - 0.5	1 / 2V _{DD}	1 / 2V _{DD} + 0.5	V
	1 / 3 Level	V _{1 / 3}	—	V _{DD} = 5V COM1~COM3, S ₀ ~S ₃₉	1 / 3V _{DD} - 0.5	1 / 3V _{DD}	1 / 3V _{DD} + 0.5	V
	2 / 3 Level	V _{2 / 3}	—	V _{DD} = 5V COM1~COM3, S ₀ ~S ₃₉	2 / 3V _{DD} - 0.5	2 / 3V _{DD}	2 / 3V _{DD} + 0.5	V
Output Current	“H” Level	I _{OH1}	—	V _{DD} = 5V, V _{OH} = 4.5V, T ₀ ~T ₅ COM1 ~COM3, S ₀ ~S ₃₉ , DATA	- 0.5	- 3.0	—	mA
	“L” Level 1	I _{OL1}	—	V _{DD} = 5V, V _{OL} = 0.5V COM1~ COM3, S ₀ ~S ₃₉ , DATA	0.5	3.0	—	mA
	“L” Level 2	I _{OL2}	—	V _{DD} = 5V, V _{OL} = 1.0V, $\overline{\text{OT0}} \sim \overline{\text{OT3}}$	10	20	—	mA
OFF-LEAK Current		I _{LO}	—	$\overline{\text{OT0}} \sim \overline{\text{OT3}}$	—	~	± 1.0	μA
N-ch Output Load Resistor		R _{ON}	—	Ta = 25°C, T ₀ ~T ₅	75	150	300	kΩ
Pull-Down Resistor		R _{IN}	—	Ta = 25°C, K ₀ ~K ₃				

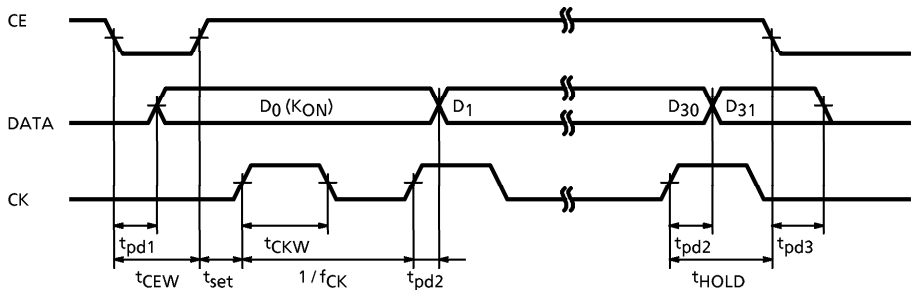
CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency	f_{OSC}	—	—	—	5	20	kHz
Operating Clock Frequency Range	f_{CK}	—	Refer to timing chart as below	—	~	2.0	MHz
Clock Pulse Width	t_{CKW}			250	~	—	ns
Data Set Time	t_{set}			250	~	—	
Data Hold Time	t_{HOLD}			250	~	—	
CE Pulse Width	t_{CEW}			250	~	—	

CE, CK, DATA-IN TIMING



CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Clock Frequency Range	f_{CK}	—	Refer to timing chart as below	—	~	2.0	MHz
Clock Pulse Width	t_{CKW}			250	~	—	ns
Data Delay Time	t_{pd1}			—	~	250	
	t_{pd2}			—	~	250	
	t_{pd3}			—	~	250	
CE Pulse Width	t_{CEW}			250	~	—	
Data Set Time	t_{set}			250	~	—	
Data Hold Time	t_{HOLD}			250	~	—	

CE, CK, DATA-OUT TIMING



QFP60-P-1414-0.80D

18.9±0.3

14.0±0.2

45

31

1.4TYP

46

30

14.0±0.2

18.9±0.3

60

16

1

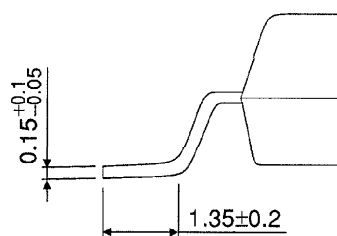
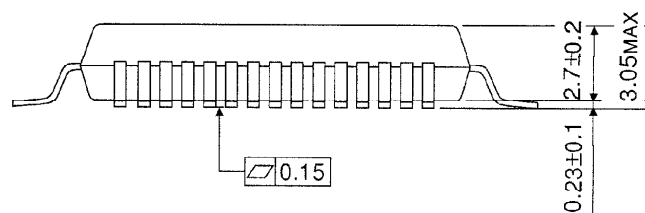
15

1.4TYP

0.35±0.1

0.8

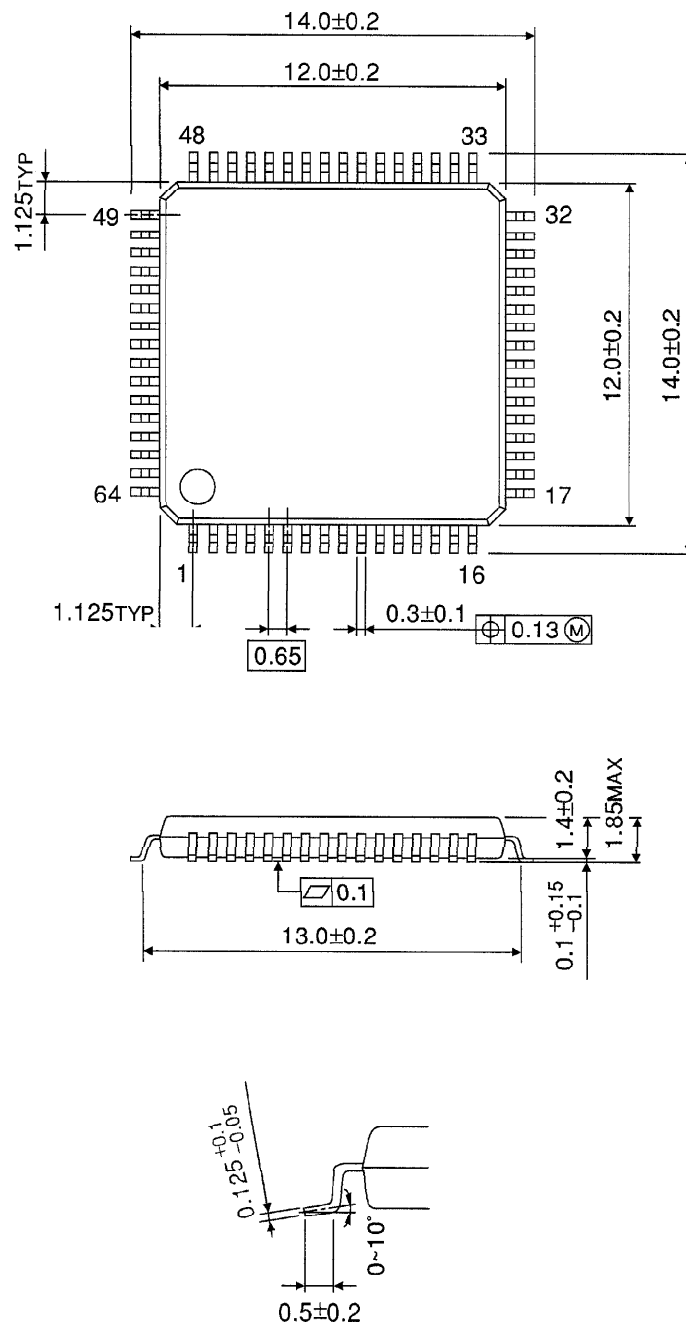
0.16 (M)



1997-06-06 16/17

OUTLINE DRAWING
QFP64-P-1212-0.65

Unit : mm



Weight : 0.45g (Typ.)