

NOT RECOMMENDED FOR NEW DESIGNS

January 1998

**High Speed CMOS Logic
Octal Bus Transceiver/Register, Three-State**

Features

- Independent Registers for A and B Buses
- CD74HC646 Non-Inverting
- CD74HC648 Inverting
- Three-State Outputs
- Drives 15 LSTTL Loads
- Typical Propagation Delay = 12ns (A to B, B to A) at $V_{CC} = 5V, C_L = 15pF, T_A = 25^\circ C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

Description

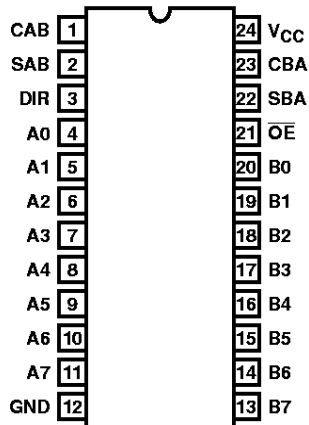
The Harris CD74HC646 and CD74HC648 are octal bus transceivers/registers with three-state non-inverting outputs. The Harris CD74HC648 is an octal bus transceiver/register with three-state inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Outputs enable (\overline{OE}) and direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the output enable (\overline{OE}) is LOW. In the high impedance mode (output enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the direction (DIR) and output enable (\overline{OE}) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE	PKG. NO.
CD74HC648EN	-55 to 125	24 Ld PDIP	E24.3
CD74HC646M	-55 to 125	24 Ld SOIC	M24.3
CD74HC648M	-55 to 125	24 Ld SOIC	M24.3

Pinout

CD74HC646, CD74HC648
(PDIP, SOIC)
TOP VIEW

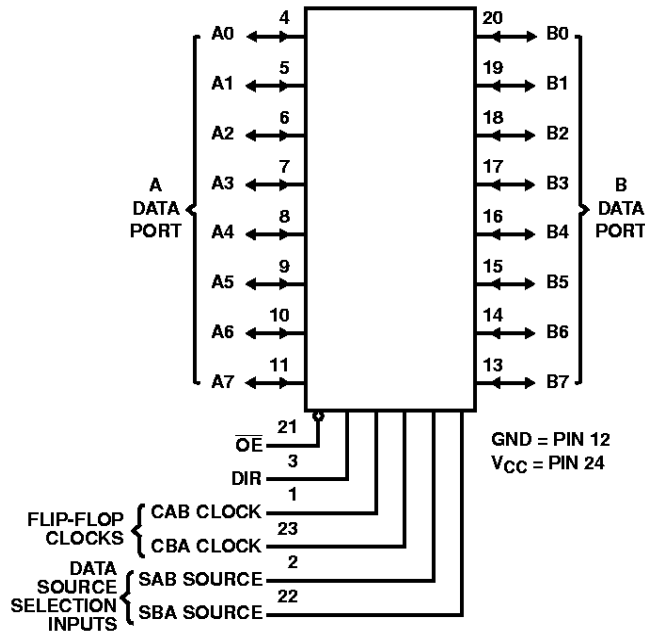


NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

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Functional Diagram



FUNCTION TABLE

INPUTS						DATA I/O (NOTE 3)		OPERATION OR FUNCTION	
\overline{OE}	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74HC646	CD74HC648
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, Hold Storage	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time \overline{B} Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored \overline{B} Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time \overline{A} Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored \overline{A} Data to B Bus

NOTE:

- The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data inputs functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs. To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10kΩ resistors.

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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	65
SOIC Package	70
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			-6	-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			6	6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA	
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	6	-	-	± 0.5	-	± 5	-	± 10	μA	

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Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Frequency	f _{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Setup Time Data to Clock	t _{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t _H	2	35	-	-	45	-	-	55	-	-	ns
		4.5	7	-	-	9	-	-	11	-	-	ns
		6	6	-	-	8	-	-	9	-	-	ns
Clock Pulse Width	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Store A Data to B Bus Store B Data to B Bus (646)	t _{PHL} , t _{PLH}	C _L = 50pF	2	-	-	220	-	275	-	330	ns
			4.5	-	-	44	-	55	-	66	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	47	-	56	ns
Store \bar{A} Data to B Bus Store \bar{B} Data to B Bus (648)	t _{PHL} , t _{PLH}	C _L = 50pF	2	-	-	240	-	300	-	360	ns
			4.5	-	-	48	-	60	-	72	ns
		C _L = 15pF	5	-	20	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	41	-	51	-	61	ns
A Data to B Bus B Data to A Bus (646)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
		C _L = 15pF	5	-	12	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	23	-	29	-	35	ns

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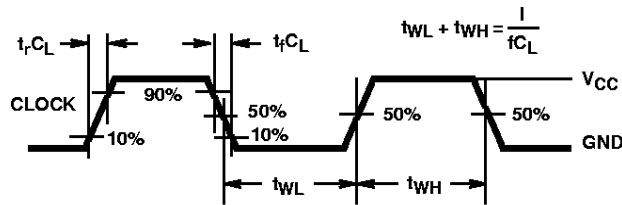
Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
A Data to B Bus B Data to A Bus (648)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	26	-	33	-	38	ns
Select to Data (646)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	29	-	37	-	43	ns
Select to Data (648)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	32	-	39	-	48	ns
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	30	-	37	-	45	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	30	-	37	-	45	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
		$C_L = 50\text{pF}$	6	-	-	10	-	13	-	15	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Maximum Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	52	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per package.
6. $P_D = V_{CC}^2 C_{PD} f_i \Sigma V_{CC}^2 C_L f_o$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

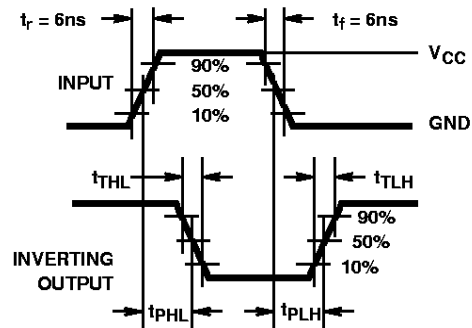


FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

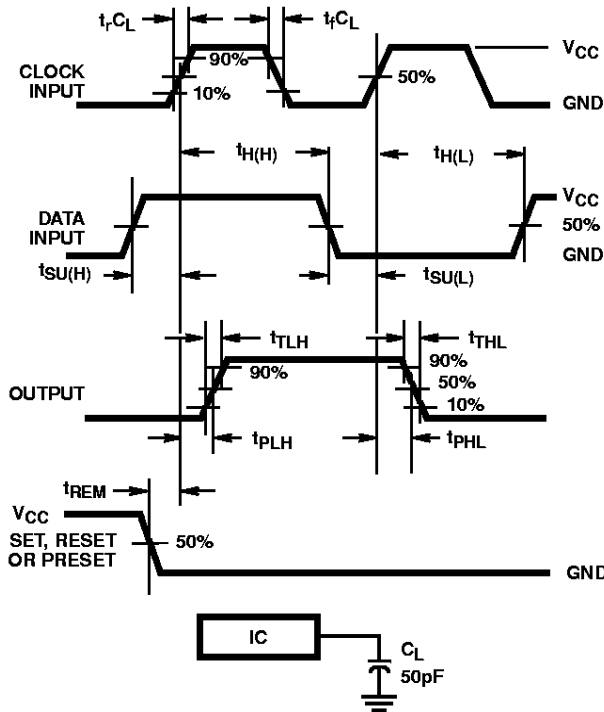


FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

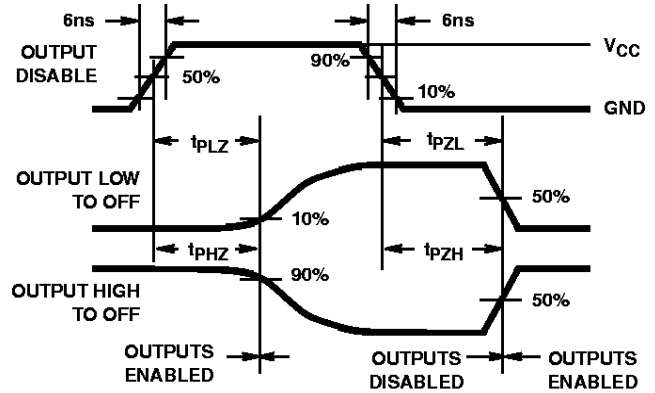
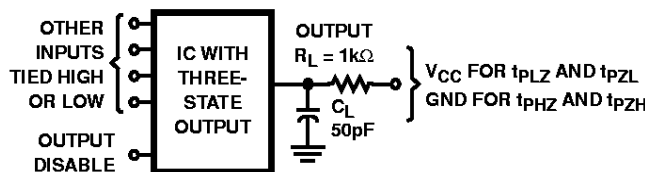


FIGURE 4. HC THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 5. HC THREE-STATE PROPAGATION DELAY TEST CIRCUIT