

**TBA950-2 Television Signal Processing Circuit**

**General Description**

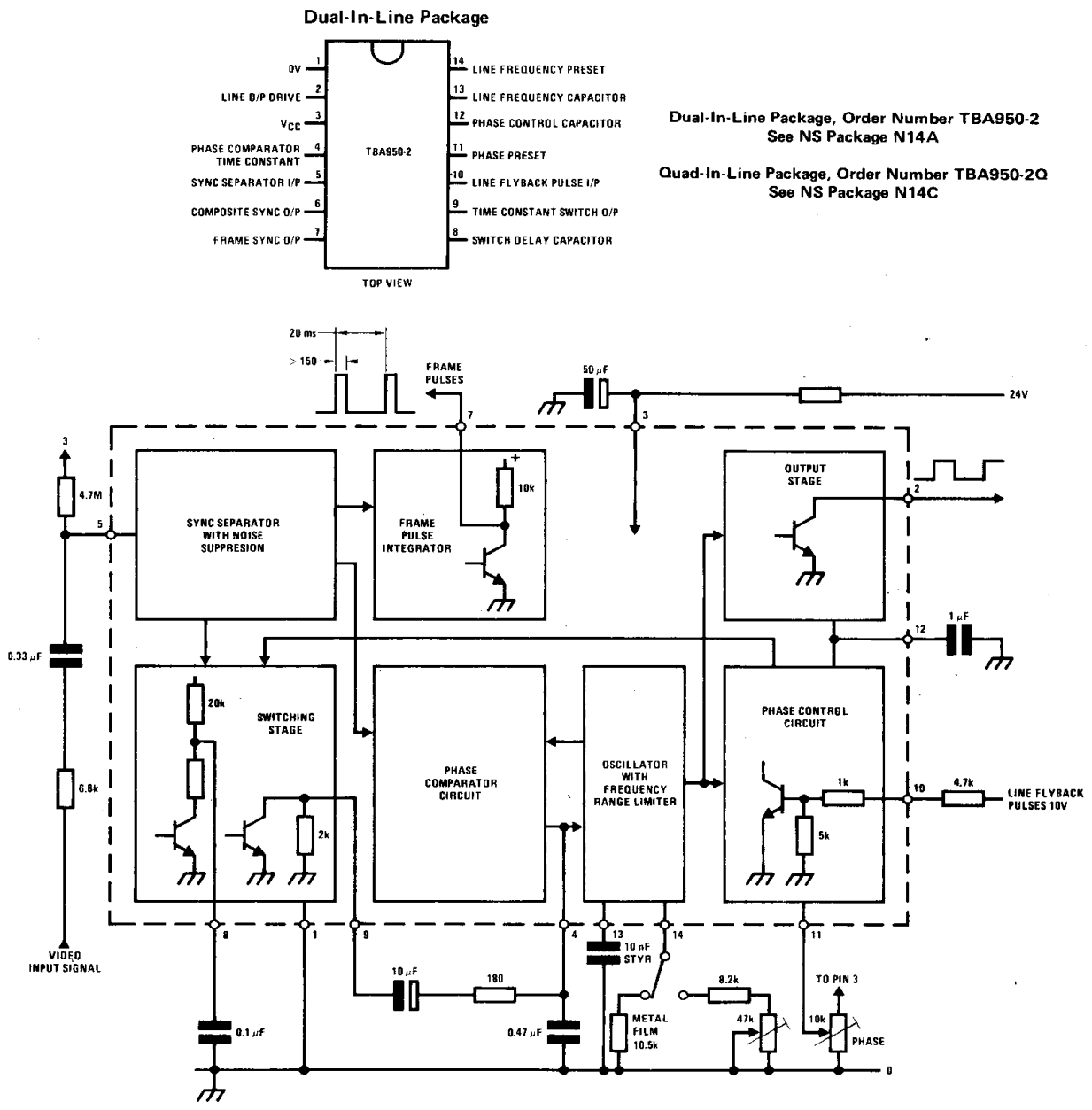
The TBA950-2 is a monolithic integrated circuit for pulse separation and line synchronization in TV receivers with transistor output stages.

noise immunity, the line oscillator with frequency-range limiter, a phase control circuit and the output stage.

The TBA950 comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of

It delivers prepared frame sync pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration, few external components are needed.

**Connection and Block Diagrams**



## Absolute Maximum Ratings

All voltages are referred to pin 1

$I_3$ , Supply Current (Figure 6)	45 mA
$I_5$ , Input Current	2 mA
$V_5$ , Input Voltage	-6V
$I_2$ , Output Current	22 mA
$V_2$ , Output Voltage	12V
$I_8$ , Switch-Over Current for Video Recording	5 mA
$I_{10}$ , Flyback Peak Pulse Current	5 mA
$V_{11}$ , Phase Correction Voltage	0 to V3
$T_A$ , Ambient Temperature	60°C

## Recommended Operating Conditions

(For operating circuits Figures 4 and 5)

$I_5$ , Input Current During Sync Pulse	> 5 $\mu$ A
$V_{IN}$ p-p, Composite Video Input Signal	3 (1 to 6)V
$I_{10}$ , Input Current During Line Flyback Pulse	0.2 to 2 mA
$I_8$ , Switch-Over Current	> 2 mA
$t_d$ , Time Difference Between the Output Pulse at Pin 2 and the Line Flyback Pulse at 10	< 20 $\mu$ s
$I_3$ , Current Consumption (Figure 6)	$\leq$ 45 mA
$T_A$ , Ambient Operating Temperature Range	0°C to +60°C

## Electrical Characteristics $T_A = 25^\circ\text{C}$ , $f_0 = 15,625$ Hz in the test circuit Figure 2 (Note 1)

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
V7	Amplitude of the Frame Pulse			>8		V
t7	Frame Pulse Durations			>150		$\mu$ s
R <sub>OUT 7</sub>	Output Resistance at Pin 7 (High State)		7.5	10	13	k $\Omega$
t2	Output Pulse Duration	Typical Ranges	25		28	$\mu$ s
V2 Res	Residual Output Voltage	$I_2 = 20$ mA		<0.55		V
$f_0$	Oscillator Frequency	C13/1 = 10 nF, R14/1 = 10.5 k $\Omega$	14063	15625	17187	Hz
$\pm\Delta f_F$	Frequency Pull-In Range		400		1000	Hz
$\pm\Delta f_H$	Frequency Holding Range	Typical Ranges	400		1000	Hz
$df_0/dt_d$	Slope of Phase Comparator Control Loop			2		kHz/ $\mu$ s
$dt_d/dt_p$	Gain of Phase Control			20		
$t_p$	Phase Shift Between Leading Edge of Composite Video Signal and Line Flyback Pulse (Note 2) Adjustable by V11	Typical Range	0		3.5	$\mu$ s

**Note 1:** By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.

**Note 2:** The limited flyback pulse should overlap the video signal sync pulse on both edges.

## Functional Description

The sync separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The RC network, hitherto required between sync separator and frame oscillator is no longer needed. Since the frame sync pulse duration at pin 7 is subject to production spreads, it is recommended to use the leading edge of this pulse for triggering.

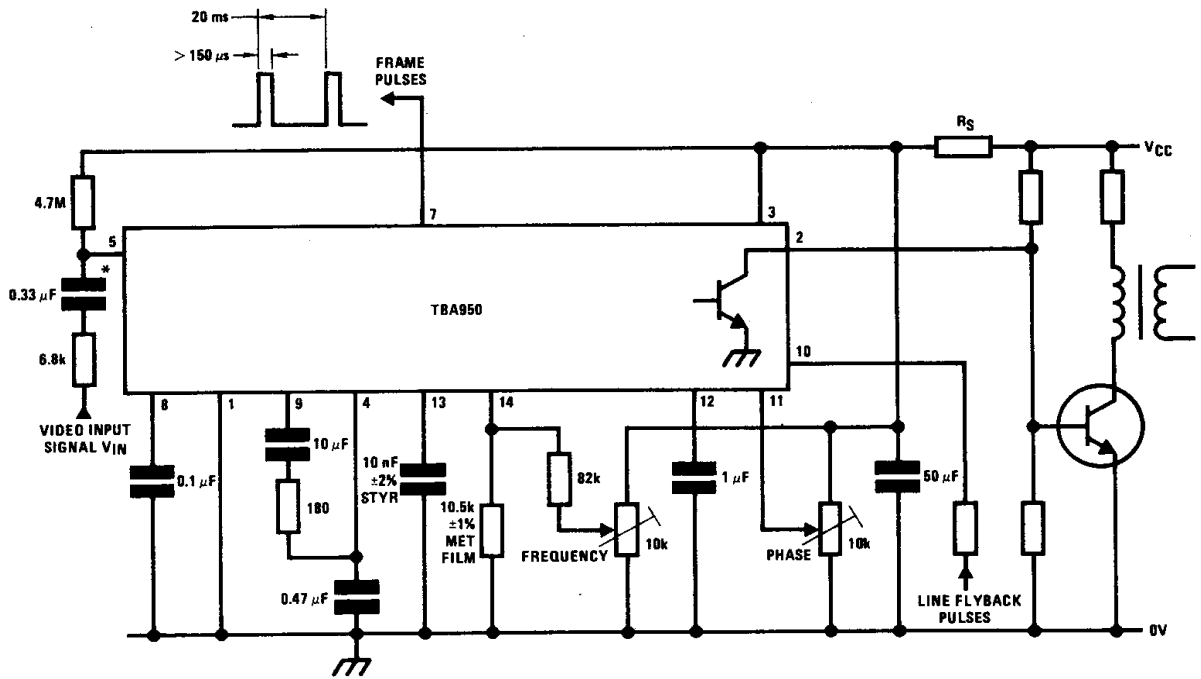
The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by 2 internal current sources. The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulses. Simultaneously, an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 k $\Omega$  potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g., due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync pulse on both edges (Figure 3).



Functional Description (Continued)



\*Input circuitry must be optimized

FIGURE 5. Another Possibility for Line Frequency Adjustment (Transistor Output Stage)

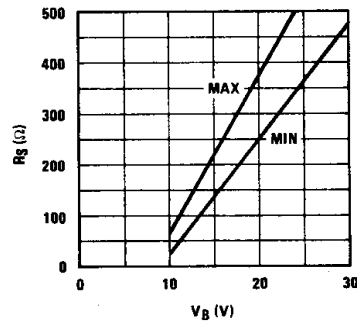


FIGURE 6. Graph for Determining the Supply Series Resistor, R<sub>S</sub>