

# TA8207K

## Low Frequency Power Amplifier

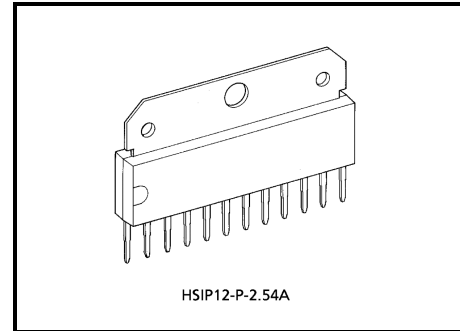
TA8207K is an audio power IC with built-in two channels developed for portable radio cassette tape recorder with power on / off switch.

Because of the parts reduction and SIP (single inline package), space merit is remarkable.

Thermal shut down protection circuit is built in.

### Features

- High power:  $P_{OUT} = 2.5W$  (typ.)  
( $V_{CC} = 9V$ ,  $R_L = 4\Omega$ ,  $f = 1kHz$ ,  $THD = 10\%$ )  
 $P_{OUT} = 4.6W$  (typ.)  
( $V_{CC} = 12V$ ,  $R_L = 4\Omega$ ,  $f = 1kHz$ ,  $THD = 10\%$ )
- Low popping noise at power on
- Small quiescent current:  $I_{CCQ} = 21mA$  (typ.) ( $V_{CC} = 9V$ ,  $V_{IN} = 0$ )
- Soft clip
- Built-in thermal shut down protection circuit
- Best for supply voltage 9V, 12V
- Operation supply voltage range:  $V_{CC} = 6\sim 15V$



Weight: 3.2g (typ.)

**Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	20	V
Output current (peak / CH)	I <sub>O</sub> (peak)	2.5	A
Power dissipation	P <sub>D</sub>	12.5	W
Operating temperature	T <sub>opr</sub>	-20~75	°C
Storage temperature	T <sub>stg</sub>	-55~150	°C

**Electrical Characteristics**(unless otherwise specified, V<sub>CC</sub> = 9V, R<sub>L</sub> = 4Ω, R<sub>g</sub> = 600Ω, f = 1kHz, Ta = 25°C, R<sub>f</sub> = 120Ω)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Quiescent current	I <sub>CCQ</sub>	—	V <sub>IN</sub> = 0	—	21	45	mA
Output power	P <sub>OUT</sub> (1)	—	THD = 10%	2.0	2.5	—	W
	P <sub>OUT</sub> (2)	—	THD = 10%, V <sub>CC</sub> = 12V	—	4.6	—	
Total harmonic distortion	THD	—	P <sub>OUT</sub> = 0.4W / ch	—	0.2	1.0	%
Voltage gain	G <sub>V</sub> (1)	—	R <sub>f</sub> = 120Ω, V <sub>OUT</sub> = 0.775V <sub>rms</sub> (0 dBm)	43	45	47	dB
	G <sub>V</sub> (2)	—	R <sub>f</sub> = 0, V <sub>OUT</sub> = 0.775V <sub>rms</sub> (0 dBm)	—	56.5	—	
Input resistance	R <sub>IN</sub>	—	—	—	30	—	kΩ
Output noise voltage	V <sub>NO</sub>	—	R <sub>g</sub> = 10kΩ, BW = 20Hz~20kHz	—	0.3	1.0	mV <sub>rms</sub>
Ripple rejection ratio	R.R.	—	R <sub>g</sub> = 600Ω, f <sub>ripple</sub> = 100Hz	—	52	—	dB
Cross talk	C.T.	—	R <sub>g</sub> = 600Ω, アンプ 1↔2, V <sub>O</sub> = 0.775V <sub>rms</sub> (0 dBm), f = 1kHz	—	50	—	dB
Input offset voltage	V <sub>6</sub> , V <sub>7</sub>	—	—	—	30	60	mV
Stand-by current	I <sub>OFF</sub>	—	SW <sub>1</sub> →off	—	1	—	μA

**Typical DC Voltage Of Each Terminal (V<sub>CC</sub> = 9V, Ta = 25°C)**

Terminal no.	1	2	3	4	5	6	7	8	9	10	11	12
DC voltage	8.7	4.5	V <sub>CC</sub>	5.0	0.7	0.03	0.03	0.7	GND	4.5	8.7	V <sub>CC</sub>

The schematic diagram illustrates a dual-channel differential amplifier circuit. It features two input channels, IN-1 and IN-2, each with a coupling capacitor (C<sub>IN</sub>), a resistor (R<sub>f</sub>), and a capacitor (C<sub>1</sub>). The inputs are connected to two operational amplifiers, both labeled CH-1. The first op-amp (top) has its non-inverting input (+) connected to a network of capacitors (C<sub>11</sub>, C<sub>4</sub>) and resistors (R<sub>f</sub>1, 120 Ω, 45 Ω, 30 kΩ). Its inverting input (-) is connected to a network of capacitors (C<sub>2</sub>, C<sub>3</sub>) and resistors (R<sub>f</sub>2, 120 Ω, 45 Ω, 30 kΩ). The second op-amp (bottom) has its non-inverting input (+) connected to a network of capacitors (C<sub>12</sub>, C<sub>5</sub>) and resistors (R<sub>f</sub>1, 120 Ω, 45 Ω, 30 kΩ). Its inverting input (-) is connected to a network of capacitors (C<sub>2</sub>, C<sub>3</sub>) and resistors (R<sub>f</sub>2, 120 Ω, 45 Ω, 30 kΩ). The outputs of the op-amps are connected to a central control block labeled "BIAS CIRCUIT THERMAL SHUT DOWN PROTECTION CIRCUIT". The outputs of this block are connected to the outputs of the op-amps, which are then connected to the outputs OUT-1 and OUT-2. The circuit is powered by VCC1 and GND. Various capacitors (C<sub>1</sub> through C<sub>12</sub>) and resistors (R<sub>f</sub>1, R<sub>f</sub>2, 120 Ω, 45 Ω, 30 kΩ) are used throughout the circuit. A switch SW1 is also present, connected to VCC1 and the first op-amp's non-inverting input.

(\*2): The condenser between the (3) pin and the GND (C<sub>11</sub>) is for reducing pop noise when the power on / off switch (SW<sub>1</sub>) is set to on / off.

## Application Information And Application Method

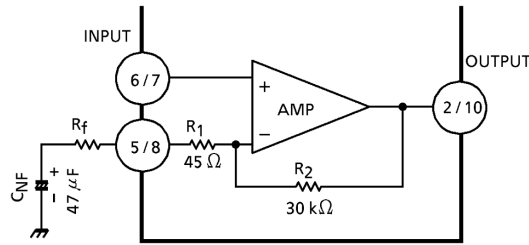
### 1. Adjustment of voltage gain

The voltage gain  $G_V$  is obtained as follows by  $R_1$ ,  $R_2$  and  $R_f$  in Fig. 1.

$$G_V = 20 \log \frac{R_f + R_1 + R_2}{R_f + R_1}$$

When  $R_f = 0\Omega$   $G_V = 56.5\text{dB}$  (typ.)

When  $R_f = 120\Omega$   $G_V = 45\text{dB}$  (typ.)



(Fig.1)

By increasing  $R_f$ , reduction of  $G_V$  is possible. However, since the feedback increase is liable to produce oscillation, it is recommended to use this at 40dB or over.

### 2. Thermal shut-down circuit

The thermal shut-down circuit is built in for the purpose of preventing the destruction of IC due to the abnormal temperature rise when the heat radiation is insufficient.

The operation temperature is set at radiation fin temperature 175°C (typ.).

At this temperature or over the bias is interrupted to prevent the destruction of IC.

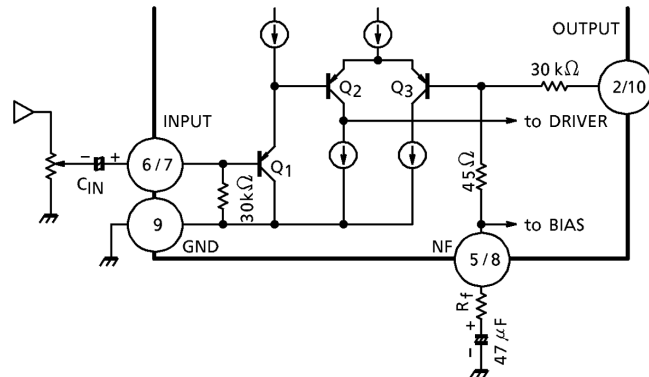
### 3. Input stage

The input circuit of this IC is as shown in Fig.2.

PNP Tr: Q1 is provided in the input circuit so as to make its usage possible without the input coupling capacitor. However, at pin(6) and (7), max 60mV offset voltage is produced.

Application after checking volume slide noise is recommended.

For cutting the volume slide noise, insert the input capacitor:  $C_{IN}$  in series to interrupt the DC component.



(Fig.2)

### 4. Oscillation preventive measures

For oscillation preventive capacitor  $C_6$  and  $C_7$  between the output terminal and GND, it is recommended to use polyester film capacitor having good characteristics for temperature and for high frequency.

Since the characteristics of the capacitor is liable to be influenced by the temperature, use this capacitor after the temperature test to check the oscillation allowance.

In addition, as the position of the electrolytic capacitor has remarkable influence on the oscillation, connect  $C_{10}$  to VCC at the nearest possible position from power GND.

At using this application with the voltage gain reduced, oscillation is liable to be produced.

Apply the capacitor after checking enough for its capacity, type and mounting position.

(\*): As the oscillation allowance varies according to the printed pattern layout, the standard printed board of TOSHIBA is recommended to be referend to design it.

## 5. Power on / off switch

There is power on / off switch at (3) pin. However, output power is changed by (3) pin supply voltage when (3) pin supply voltage is not same (12) pin supply voltage, after referring to attached date, select (3) pin supply voltage.

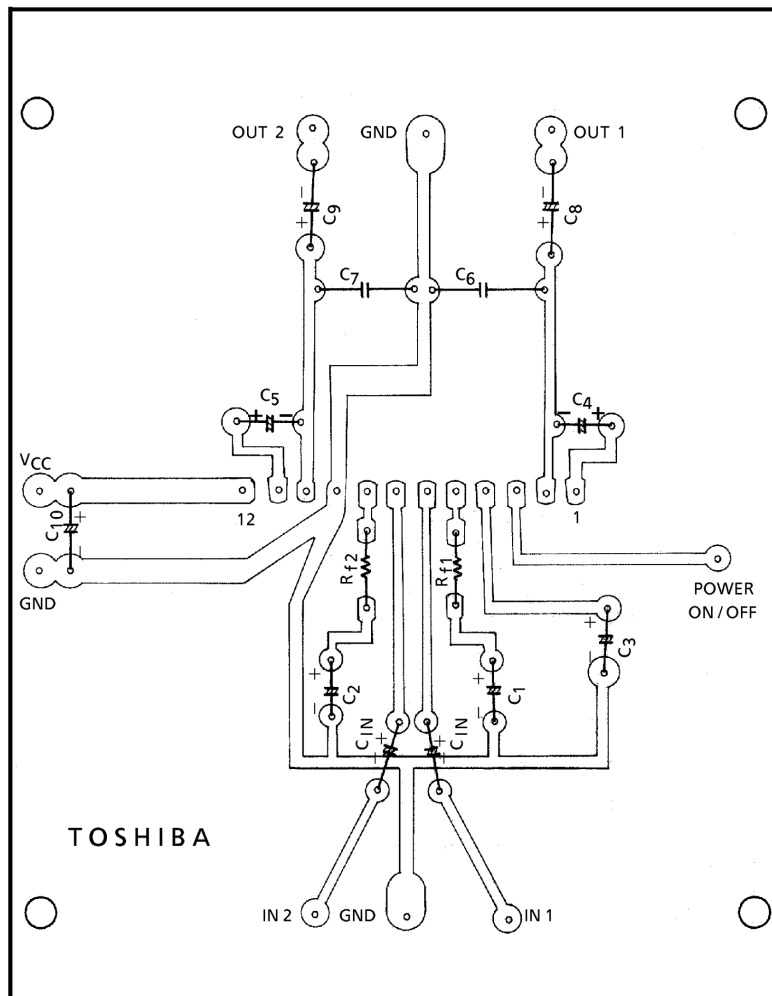
## 6. Input voltage

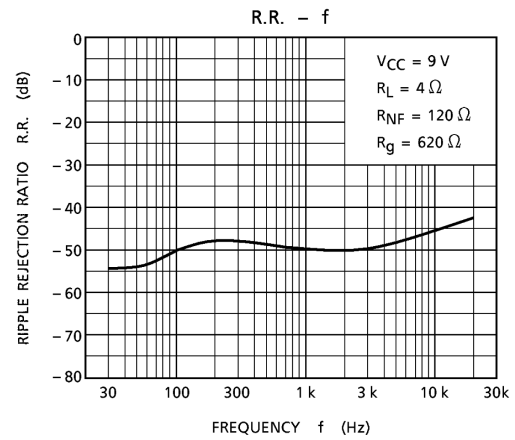
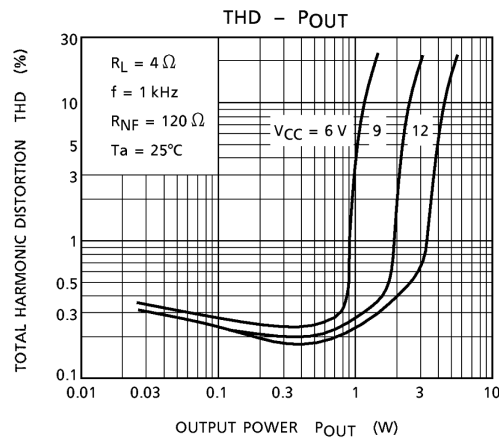
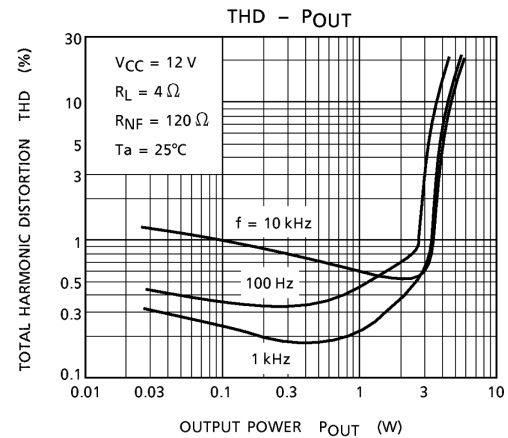
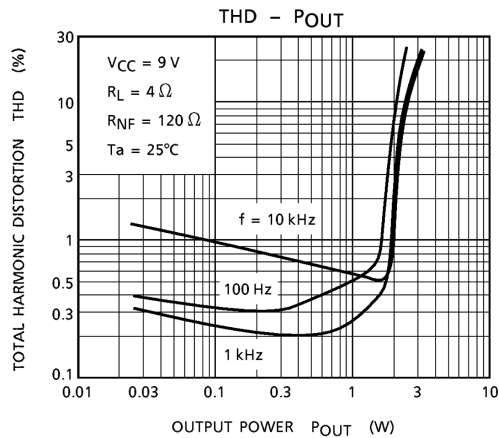
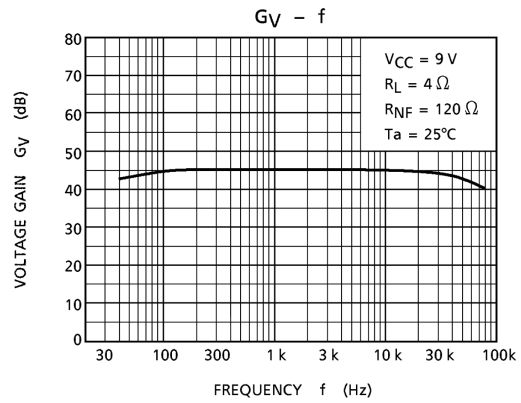
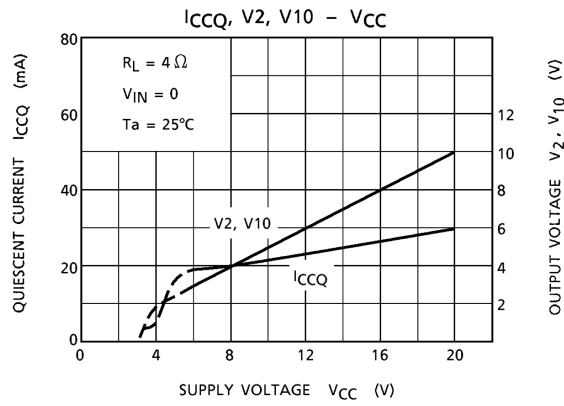
When the excessive signal is input, turning-up is produced in the clip waveform. The turning-up point is  $V_{IN} = 300mV_{rms}$  (typ.):  $V_{CC} = 9V$ ,  $R_L = 4\Omega$ ,  $f = 1kHz$ : Enough care must be taken for this phenomenon.

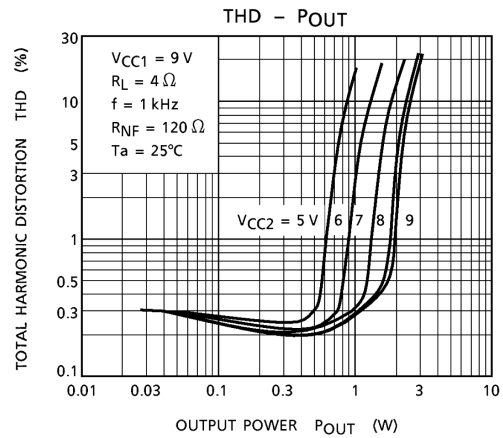
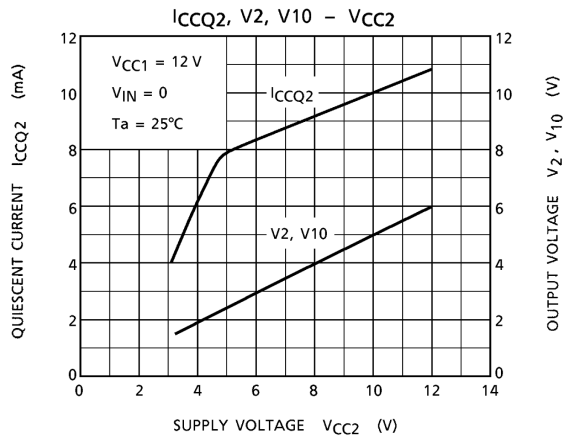
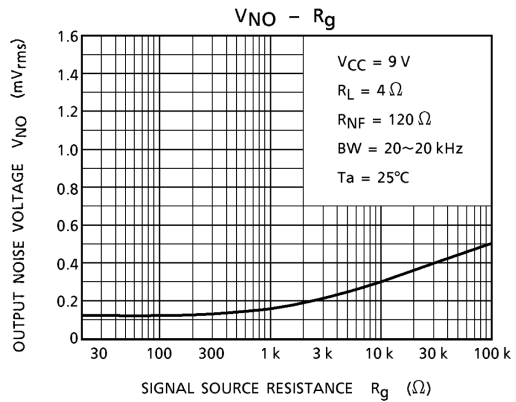
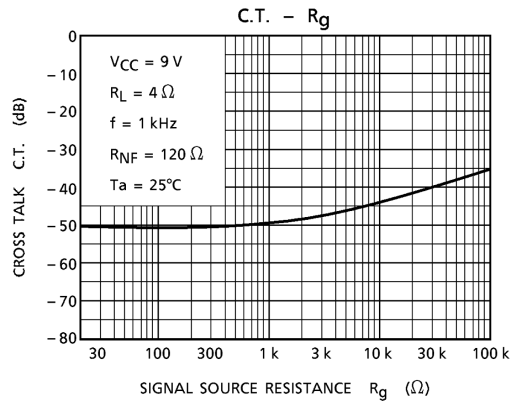
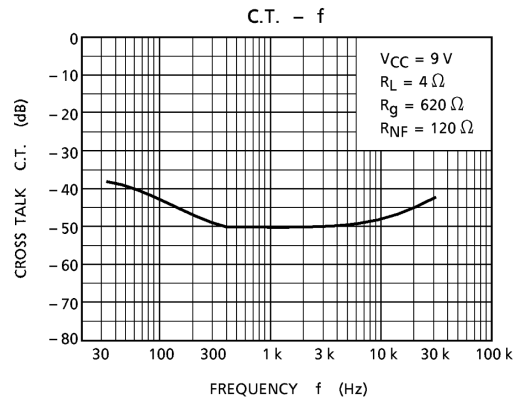
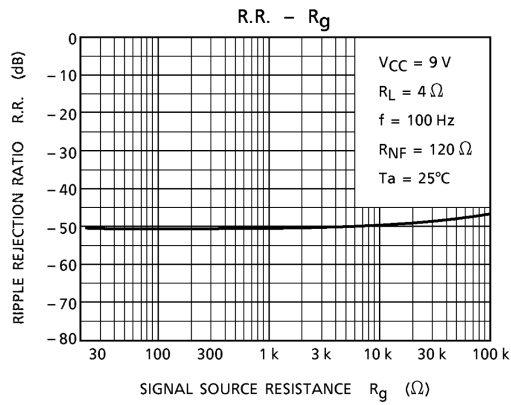
## 7. GND line

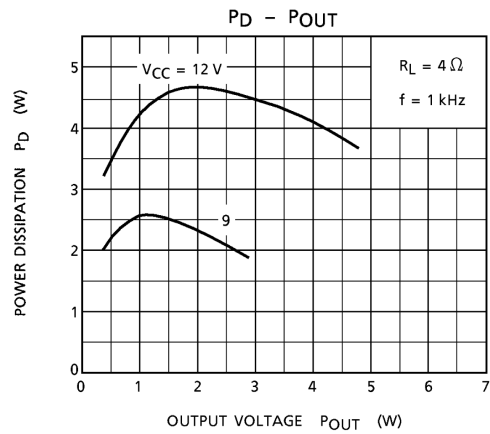
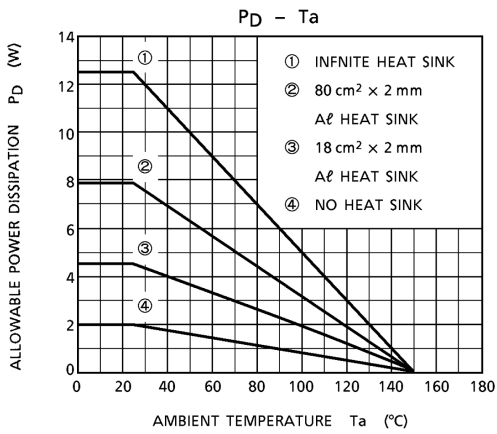
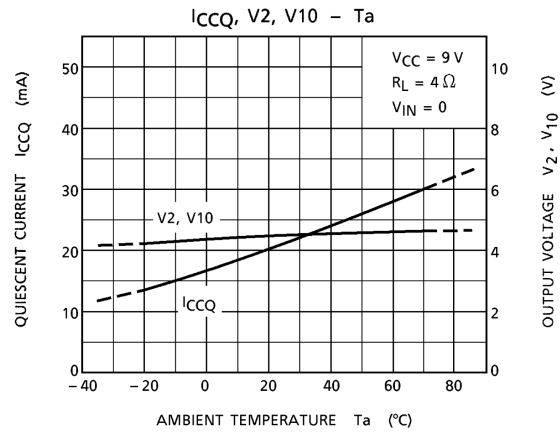
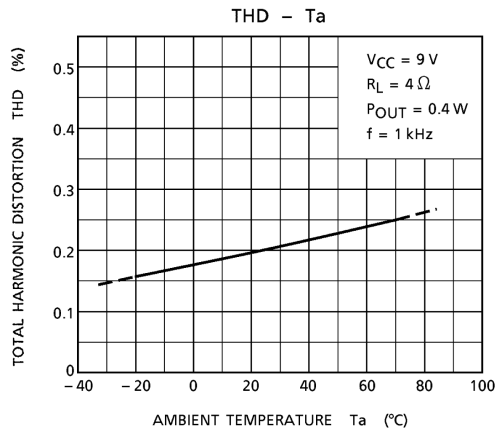
GND pin is not separated for pre-GND and for PW-GND. That is liable to cause distortion and cross talk worse. Before use this IC, please check it.

## Standard Print Pattern







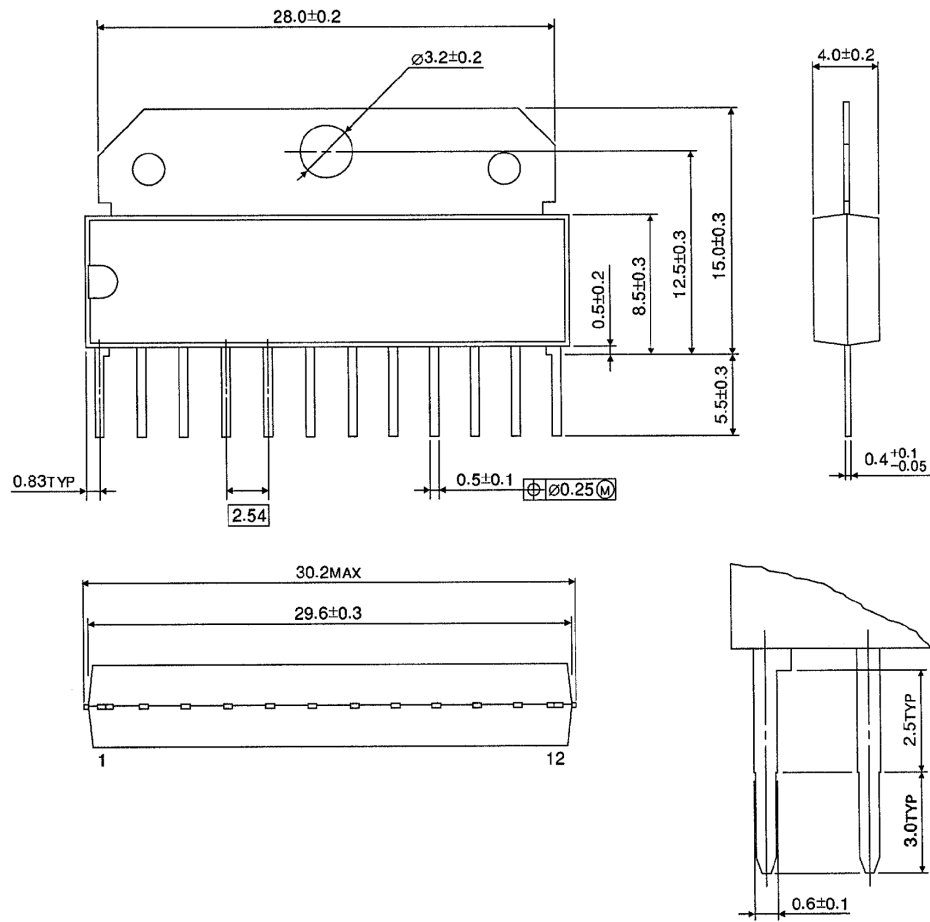




## Package Dimensions

HSIP12-P-2.54A

Unit : mm



Weight: 3.2g (typ.)

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