

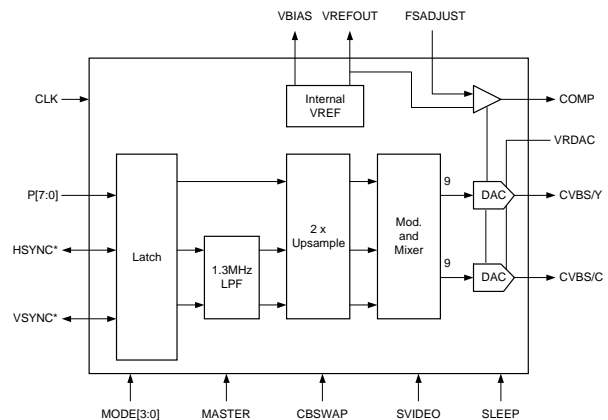
GENERAL DESCRIPTION

The SPCA711A is designed specifically for VideoCD, video games and other digital video systems, which require the conversion of digital YCrCb (MPEG) data to analog NTSC/PAL video. The device supports a glue-less interface to most popular MPEG decoders. The SPCA711A supports worldwide video standards, including NTSC (N America, Japan) PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay), and PAL-Nc (Argentina). Furthermore, the SPCA711A operates with a single 2x clock and can be powered with a single 3.3V supply. The composite analog video signal is output simultaneously onto two outputs. Therefore, it allows one output to provide base-band composite video while the other drives a RF modulator. Alternatively, analog luminance (Y) and chrominance (C) information is available for interfacing to S-video equipment. As a slave, the SPCA711A automatically detects the input data formats (PAL/NTSC, CCIR601) and switches internally to provide the proper format on the outputs. This feature, along with the on-board voltage reference and single clock interface, makes the SPCA711A extremely simple to use. In addition, use of 2x over-sampling on-chip simplifies external filter design resulting in reduced overall system cost.

FEATURES

- 8-bit 4:2:2 YCrCb inputs for glue-less interface to MPEG decoders
- NTSC/PAL/PAL-M/PAL-Nc composite video outputs
- CVBS or S-video outputs
- 3.3 V supply voltage
- CCIR 601 operation
- 2x over sampling simplifies external filtering
- 9-bit DACs
- Master or slave video timing
- Interlaced operation
- Automatic mode detection/switching in slave mode
- On-board voltage reference
- 27MHz crystal oscillator input
- 32-pin PLCC package

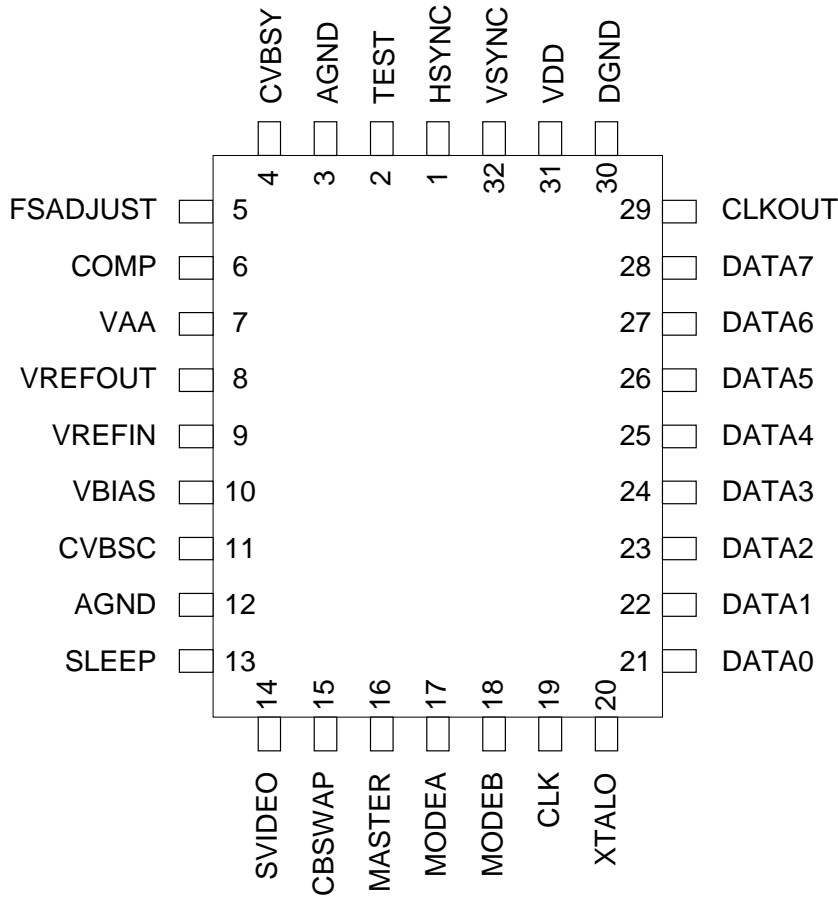
BLOCK DIAGRAM



APPLICATIONS

- VideoCD
- Karaoke/video games
- Digital Video Disk (DVD)
- Digital VCR
- Digital set top box

PINOUT and DESCRIPTION



(Table 1.)

Mnemonic	PIN No.	Type	Description
DATA[7:0]	21 - 28	I	YCrCb pixel inputs. They are latched on the rising edge of CLK. YCrCb input data conform to CCIR 601.
CLKOUT	29	O	Pixel clock output
VSYNC	32	I/O	Vertical sync input/output. VSYNC is latched/output following the rising edge of CLK.
HSYNC	1	I/O	Horizontal sync input/output. HSYNC is latched/output following the rising edge of CLK.
MASTER	16	I	Master/slave mode selection. A logical high for master mode operation. A logical 0 for slave mode operation.
CBSWAP	15	I	Cr and Cb pixel sequence configuration pin. A logic high swap the

Mnemonic	PIN No.	Type	Description
			Cr and Cb sequence.
SVIDEO	14	I	SVIDEO select input pin. A logic high selects Y/C output. A logic low selects composite video output.
SLEEP	13	I	Power save mode. A logic high on this pin puts the chip into power-down mode. This pin is equal to reset pin. An external logic high pulse should input to the pin when power on.
MODEA	17	I	Mode configuration pin.
MODEB	18	I	Mode configuration pin.
CLK	19	I	27MHz crystal oscillator input. A crystal with 27MHz clock frequency can be connected between this pin and XTALO.
XTALO	20	O	Crystal oscillator output.
TEST	2	I	Test pin. These pins must be connected to DGND.
VREFIN	9	I	Voltage reference input. An external voltage reference must supply typical 1.235V to this pin. A 0.1 μ F ceramic capacitor must be used to de-couple this input to GND. The decoupling capacitor must be as closed as possible to minimize the length of the lead. This pin may be connected directly to VREFOUT.
VREFOUT	8	O	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive VREFIN pin directly.
FSADJ	5	-	Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground.
COMP	6	-	Compensation pin. A 0.1 μ F ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
VBIAS	10	-	DAC bias voltage. Potential normally 0.7V less than COMP.
VDD	31	-	Digital power pin
DGND	30	-	Digital ground pin
CVBSY	4	O	Composite/Luminance output. This is a high-impedance current source output. The output format can be selected by the PAL pin. The CVBSY can drive a 37.5 Ω load.
CVBSC	11	O	Composite/Chroma output. This is a high impedance current source Output. The output format can be selected by the PAL pin. The pin can drive a 37.5 Ω load.

Mnemonic	PIN No.	Type	Description
VAA	7	-	Analog power pin
AGND	3,12	-	Analog ground pin

MODE SELECTION

The master mode is selected when MASTER = 1; slave mode is selected when MASTER = 0. Two pins, MODEA, MODEB, drive three different configuration registers. The most common operating modes can be selected with these pins while in the master mode. In the slave mode, as well as the common operating modes, are automatically determined from the timing of the incoming HSYNC* and VSYNC* signals.

NOTE: The term “common operating mode” refers to the North American NTSC and Western European PAL. **Table 2** illustrates the multi-functionality of the mode pins in the master and slave mode. To access the more exotic video formats, slave mode is preferred since the necessary registers are always accessible. If the master mode is needed, the less common modes can still be programmed by first registering the modes as slave and then switching to a master. During power-up, the MODE [3:2] pins configure the master registers, i.e., EFIELD and PAL625 are written. Also, during power-up, the slave registers are reset to zero, i.e., YCSWAP.

Table 2. Mode Selection

The MASTER pin	PIN Description	
	MODEA	MODEB
0	YCSWAP	PALSA
1	EFIELD	PAL625

Table 3. Configuration Register Settings

Mode Register Name	Set to 0	Set to 1	Comments
EFIELD	The VSYNC pin will output normal vertical synchronization signals.	The VSYNC pin will output field signals. Low at the VSYNC pin for an even field, high for odd field.	This is only used in the master mode.
PAL625	The 525-line operation will be selected.	The 625-line operation will be selected	This is only used in the master mode
YCSWAP	Do not swap Y and Cr/Cb Sequence.	Swap Y and Cr/Cb sequence.	----
PALSA	When the PAL625 register is set to high, the PAL-BDGHl mode is selected. When the PAL625 register is set to low, the NTSC mode is selected.	When the PAL625 register is set to high, the PAL-Nc mode is selected. When the PAL625 register is set to low, the PAL-M mode is selected.	---

CLOCK TIMING

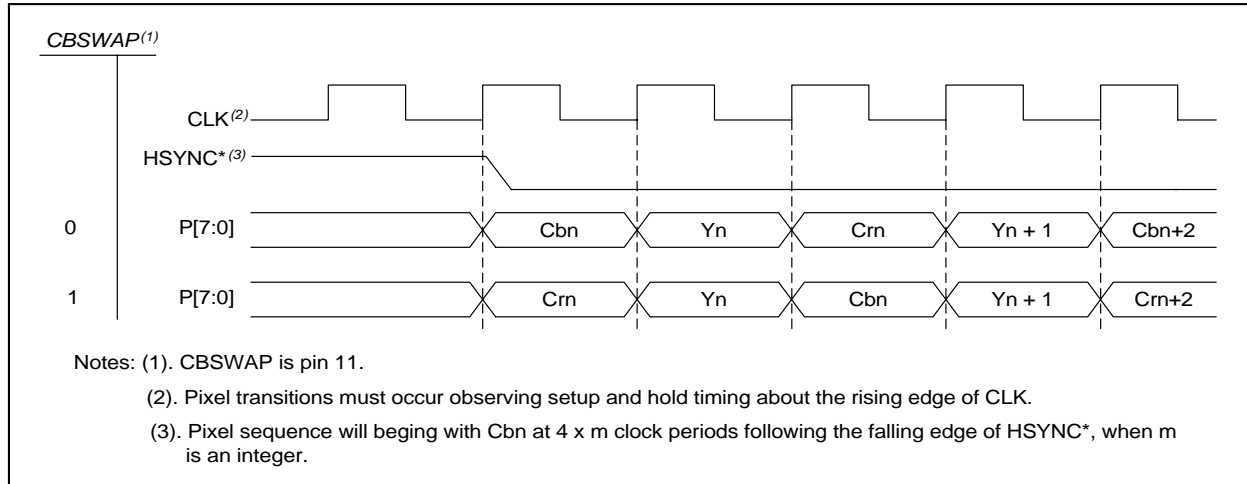
A clock signal with a frequency of twice the luminance sampling rate must be present at the CLK pin. All setup and hold timing specifications are measured with respect to the rising edge of this signal.

PIXEL INPUT TIMING

■ PIXEL SEQUENCE

Multiplexed Y, Cb, and Cr data is input through the DATA[7:0] inputs. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR-656. This pattern begins during the first CLK period after the falling edge of HSYNC* (regardless of the setting of SLAVE/MASTER mode). Cb and Cr order can be reversed by setting the CBSWAP pin. **Figure 1** illustrates the timing. If the pixel stream input to the SPCA711A is off by one CLK period, the SPCA711A can lock to the pixel stream by setting the YCSWAP register. This will prevent Y and Cr/Cb pixels from swapping.

Figure 1. Pix Sequence



VIDEO TIMING

The width of analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR-624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, and the burst envelope are internally controlled. Video timing figures follow the guidelines given in this section.

■ SYNC AND BURST TIMING

Table 4 lists the resolutions and clock rates for the various modes of operation.

Table 5 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked. The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync. The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level). The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level).

Table 4. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active pixels	Total Pixels	CLK Frequency (MHz)
NTSC/PAL-M CCIR601	720 x 240	858 x 262	27
PAL-B,D,G,H,I, Nc	720 x 288	864 x 313	27

Table 5. Horizontal Counter Values for Various Video Timings

Operation Mode	Front porch (a)	Horizontal Sync Width (b)	Start of Burst (c)	Duration of Burst (d)	Back porch (e)
NTSC CCIR601	20	63	72	34	127
PAL-B CCIR601	20	63	76	30	142

Notes: (1) The unit are in number of luminance pixels.

■ MASTER MODE

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, and VSYNC* are output following the rising edge of CLK. The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line. The vertical counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation, it is reset to one, indicating the start of a new field. VSYNC* is asserted for 3 or 2.5 scan lines for the 262/525 line and the 312/625 line, respectively.

■ SLAVE MODE

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of the CLOCK. The horizontal counter is incremented on the rising edge of the CLOCK. Two clock cycles after falling edge of HSYNC*, the counter is reset to one, indicating the start of a new line. The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field. A falling edge of VSYNC* occurring within $\pm 1/4$ of a scan line from the falling edge of HSYNC* cycle time (line time) indicates the beginning of Field 1. A falling edge of VSYNC* occurring within $\pm 1/4$ scan line from the mid-point of the line indicates the beginning of Field 2.

The operating mode (NTSC/PAL) can be programmed with the MODEA and MODEB bits when the SETMODE (MASTER pin) bit is set high. Alternatively, when the SETMODE bit is set low, the mode is automatically changed to the slave mode. For example, 525-line operation is assumed, 625-line operation is detected by the number of HSYNC* edges between VSYNC* edges. The frequency of operation (CCIR-601) for both PAL and NTSC is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz, ± 1 count and is between two successive falling edges of HSYNC*.

■ BURST BLANKING

For NTSC, color burst information is automatically disabled on scan lines 1-9 and 264-272, inclusive(SMPTE line numbering convention). For PAL-B, D, G, H, I, Nc color burst information is automatically disabled on scan lines 1-6, 310-318, and 623-625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1-5, 311-319, and 622-625, inclusive.

VERTICAL BLANKING INTERVALS

NTSC scan lines 1-9 and 263-272, inclusive, are always blanked. There is no setup on scan lines 10-21 and 273-284, inclusive. All displayed lines in the vertical blanking interval (10-21 and 273-284 for interlaced NTSC; 7-13 and 320-335 for interlaced PAL-B, D, G, H, I) are forced to blank. For PAL-B, D, G, H, I, scan lines 1-6, 311-318, and 624-625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1-5, 311-319, and 624-625, inclusive, are always blanked.

■ DIGITAL PROCESSING

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter. The Y and filtered UV components are up-sampled to CLK frequency by a digital filter.

■ SUBCARRIER GENERATION

To maintain a synchronous sub-carrier relative to HSYNC*, the sub-carrier phase is reset every frame of the NTSC and every 8 fields of the PAL. The SCA phase is non-zero and depends upon the clock frequency and the video format.

For perfect clock input, the burst frequency is 4.43361875 MHz for PAL-B, D, G, H, I, 3.57561149MHz for PAL-M, 3.58205625MHz for PAL-Nc (Argentina), 3.579545 MHz for NTSC interlaced.

■ POWER-DOWN MODE

In the power-down mode (SLEEP pin set to 1), the internal clock is stopped, an internal reset is forced, and the DACs are powered down. When returned to low, the device starts from a reset state (horizontal and vertical counters = 0, which is the start of VSYNC in Field 1). This mode should be set when the SPCA711A is subjected to clock frequencies outside its functional range. If Master = 1, the HSYNC* and VSYNC* pins remain driven to the value of previous output before SLEEP was activated. Power down current is dependent on loading to the HSYNC* and VSYNC* pins.

Figure 2. Interlaced 525-Line (NTSC) Video Timing

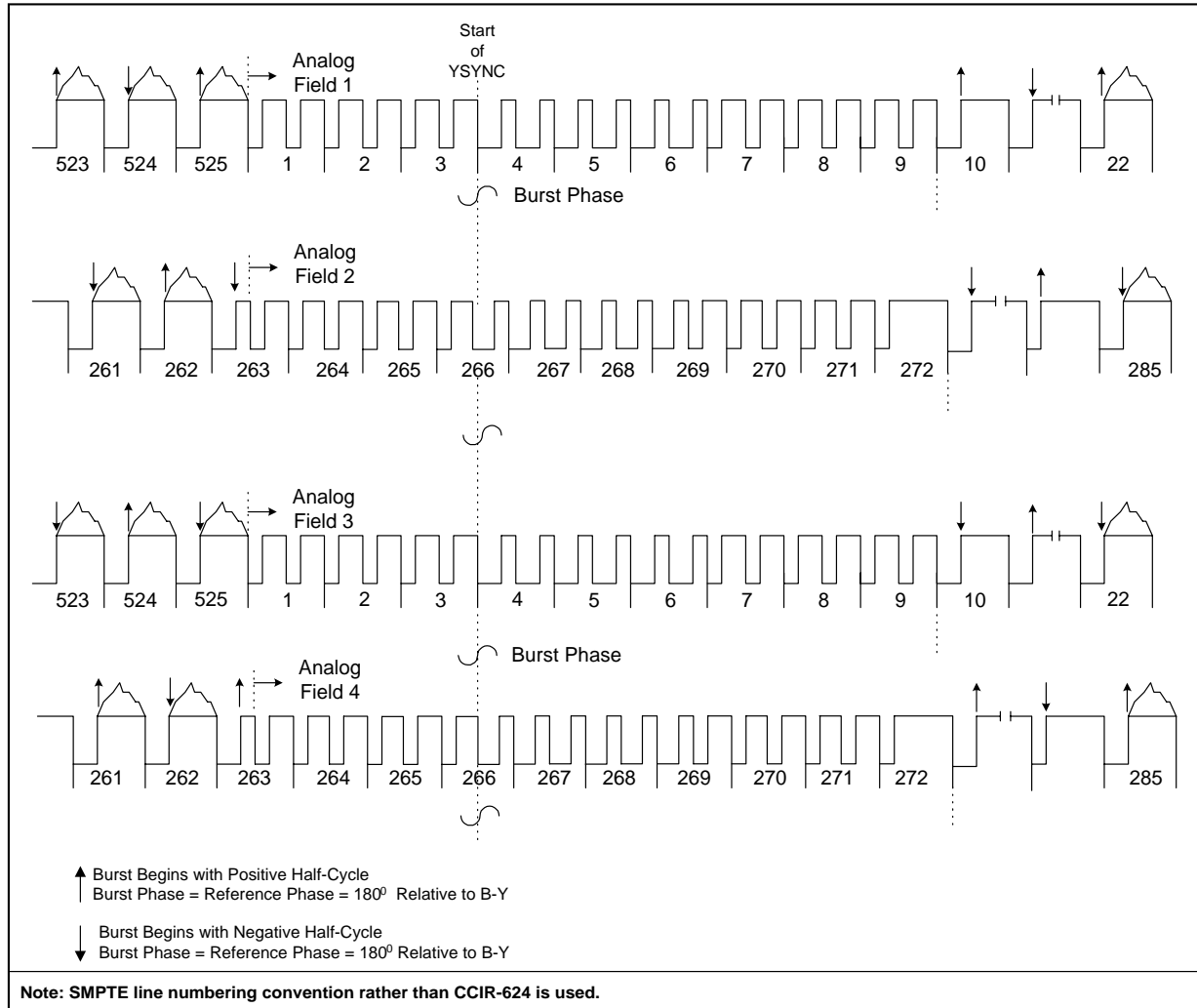


Figure 3a. Interlaced 625-Line (PAL) Video Timing

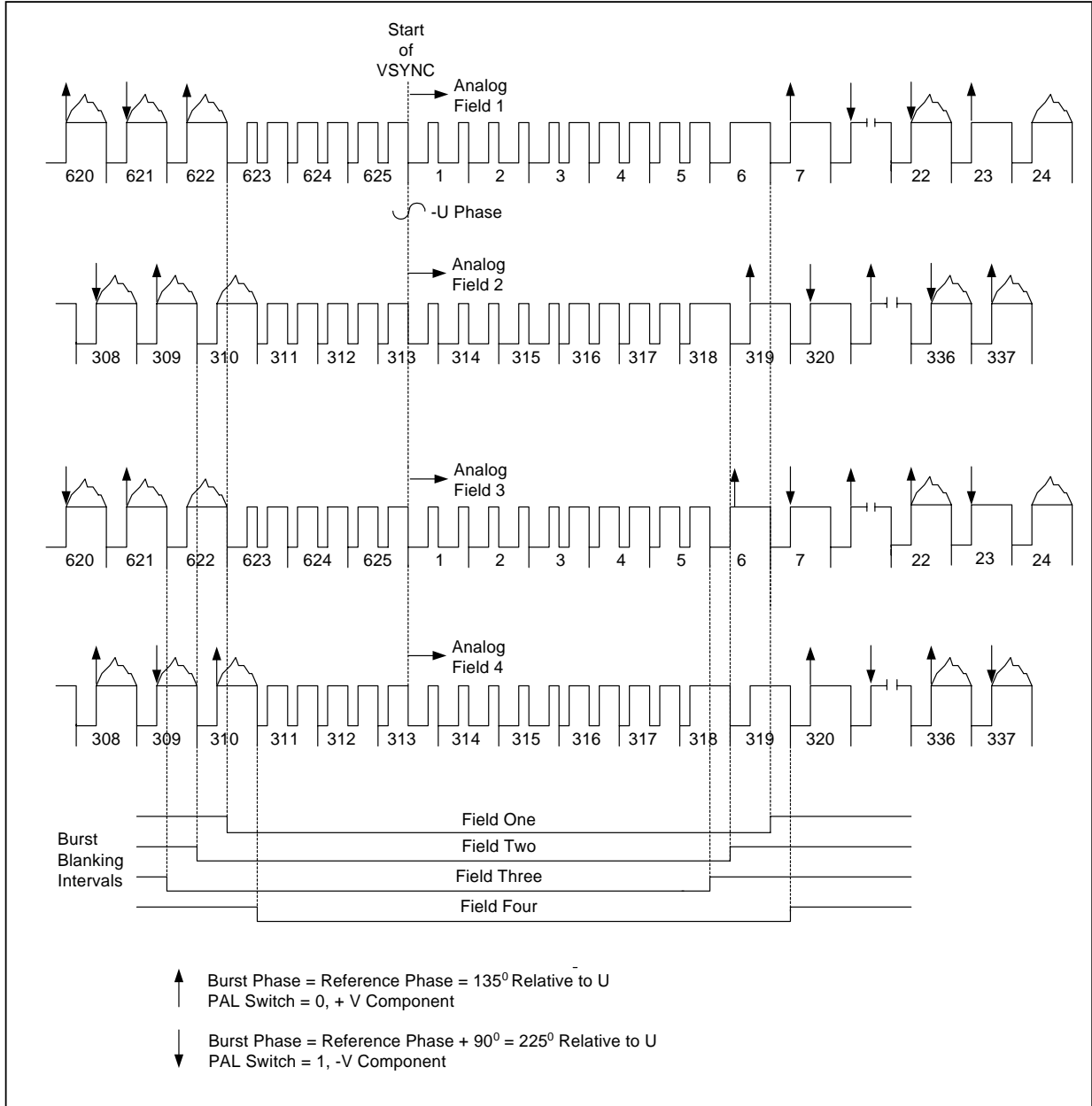
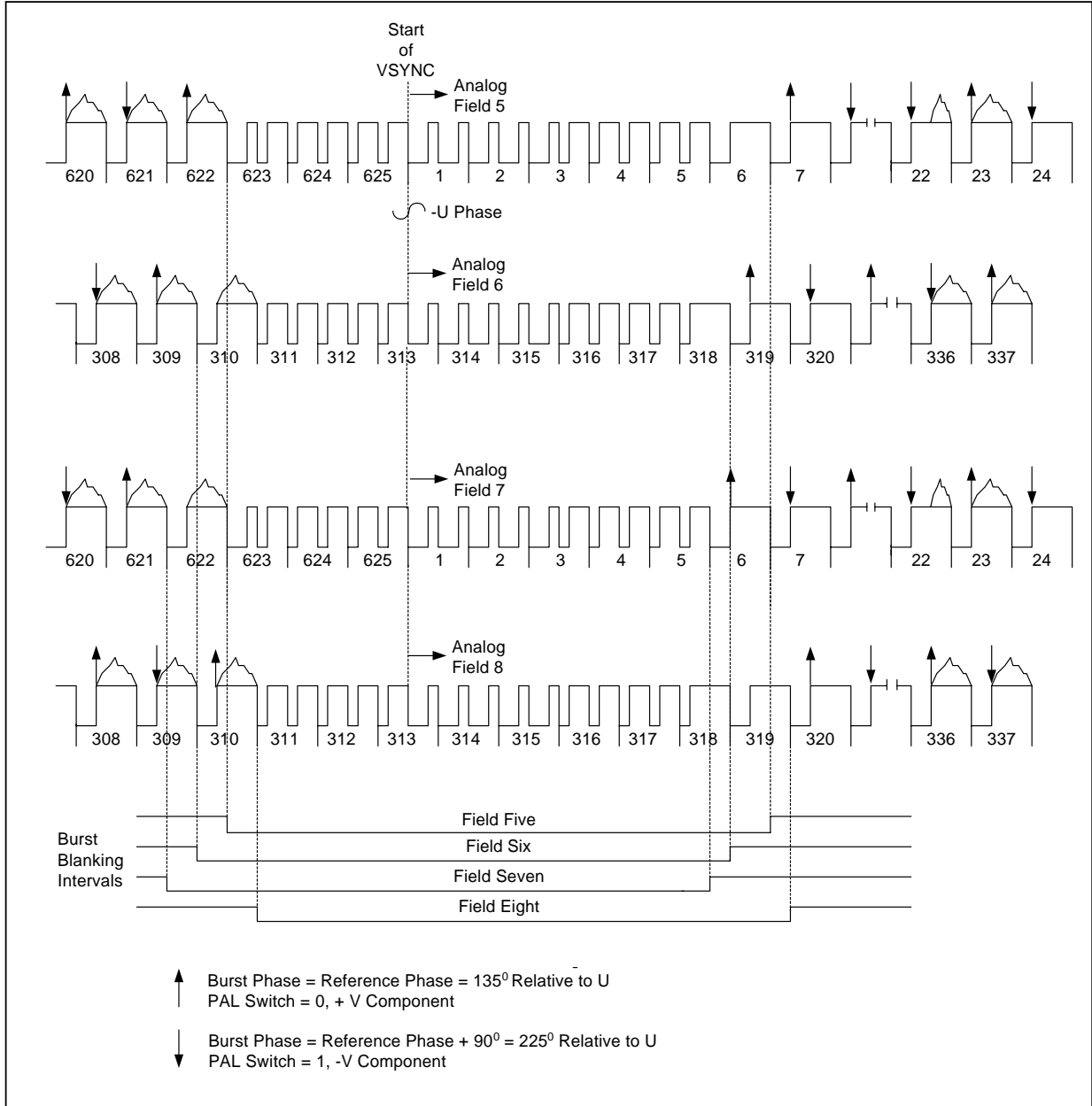


Figure 3b. Interlaced 625-Line (PAL) Video Timing



ELECTRICAL CHARACTERISTICS
■ Absolute Maximum Ratings

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply (Measured to ground)	VAA			4.5	V
Ambient Operating temperature	TA	-40		+125	°C
Voltage on Any Signal Pin		GND-0.5		VAA+0.5	V
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C

Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latch-up.

■ Recommended Operating Conditions

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply	VAA	3	3.3	3.6	V
Ambient Operating temperature	TA	0	--	+70	°C
DAC Output Load	RL	--	37.5	--	Ω
External Voltage Reference	VREFIN		1.27		V

■ DC Characteristics

Characteristics	Symbol	Limit			Unit
		Min	Typ	Max	
Analog Power Operating Voltage	V _{AA}	3.0	3.3	3.6	V
Digital Power Operating Voltage	V _{DD}	3.0	3.3	3.6	V
Operating Current	I _{OP}		90	300	mA

Power Down Mode Current			20		mA
Input High Voltage (Digital Input)	V _{IH}	2.0		V _{AA} +0.5	V
Input Low Voltage (Digital Input)	V _{IL}	GND-0.5		0.8	V
Output High I (V _{OH} =2.4V) (Digital Output)	I _{OH}		-8		mA
Output Sink I (V _{OL} =0.8V) (Digital Output)	I _{OL}		8		mA
VREFOUT Output Voltage	VREFOUT		1.27		V
VREFOUT Current	IREFOUT		10		uA

PIXEL INPUT RANGES AND COLORSPACE CONVERSION

■ YC INPUTS (4:2:2 YCRCB)

Y has a nominal range of 16-235. Cb and Cr have a nominal range of 16-240, with 128 equal to zero. Y values of 0-15 and 236-255 are interpreted as 16 and 235. CrCb values of 1-15 and 241-254 are interpreted as 16 and 240.

■ DAC CODING

White is represented by DAC code 800. For PAL-B, D, G, H, I, and Nc the standard blanking level is represented by DAC code 252. NTSC standard blanking level is represented by DAC code 240.

OUTPUTS

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Either two composite video outputs or Y/C S-Video outputs are available (selectable by the SVIDEO pin). If the SLEEP pin is high, the DACs are essentially turned off and only leakage current is present.

COMPOSITE AND LUMINANCE (CVBS/Y) ANALOG OUTPUT

When SVIDEO is a logical zero, digital composite video information drives the 9-bit D/A converter that generates the CVBS output. When SVIDEO is a logical one, digital luminance information drives the DAC that generates the analog Y video output.

■ COMPOSITE AND CHROMINANCE (CVBS/C) ANALOG OUTPUT

When SVIDEO is a logical zero, digital composite video information drives the 9-bit D/A converter that generates CVBS output. When SVIDEO is a logical one, digital chrominance information drives the 9-bit D/A converter that generates analog C video output.

PC BOARD CONSIDERATIONS

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing. A well-designed power distribution network is critical to eliminate digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

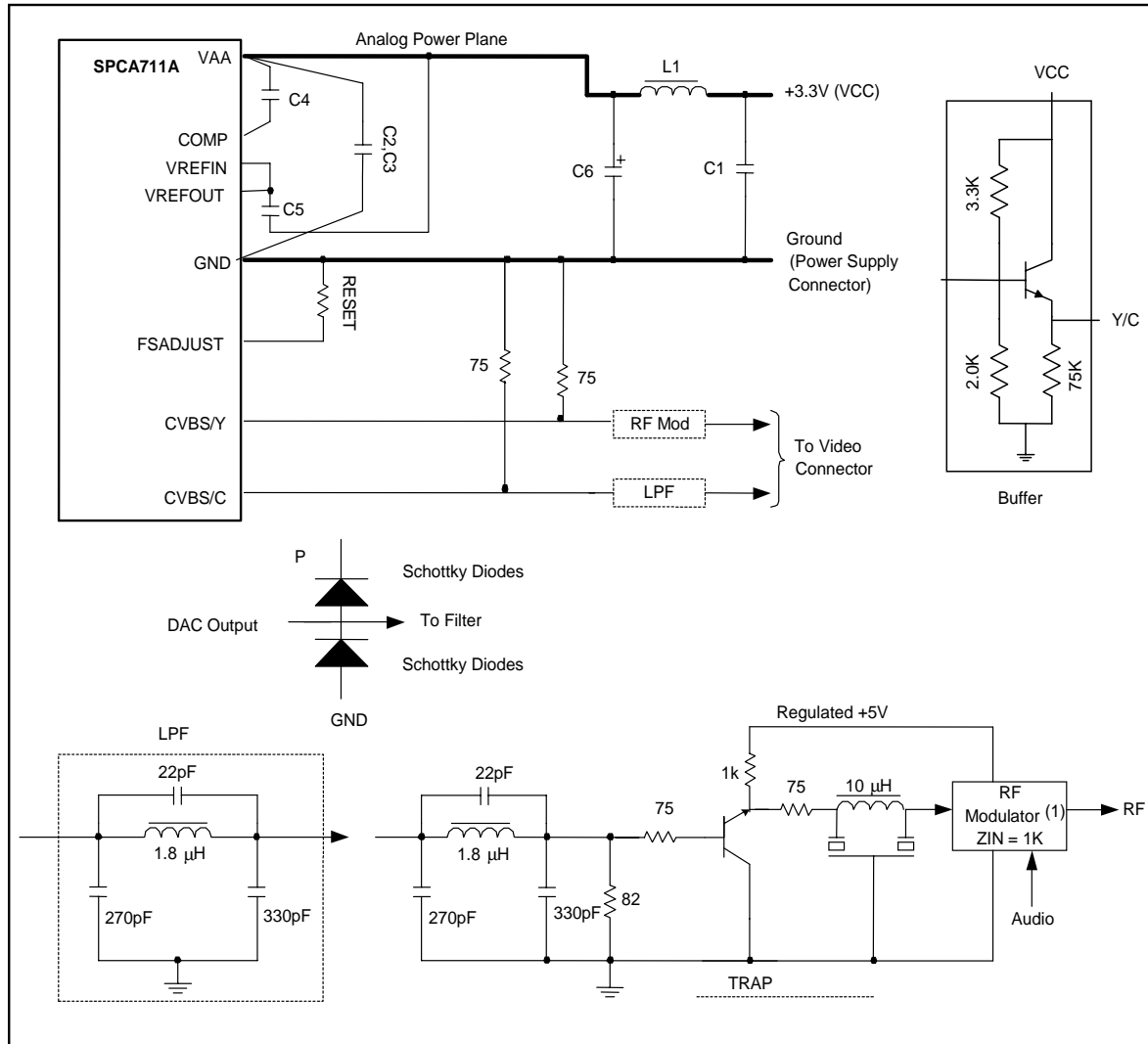
■ COMPONENT PLACEMENT

Components should be placed as close as possible to the associated pin. The optimum layout enables the SPCA711A to be located as close as possible to the power supply connector and the video output connector.

■ POWER AND GROUND PLANES

For optimum performance, a common digital and analog ground plane is recommended. Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SPCA711A power pins, VREF circuitry, and COMP decoupling. At least a 1/8-inch gap is required in between the digital power plane and the analog power plane. The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in **Figure 4, Table 6**. This bead should be located within 3 inches of the SPCA711A. The bead provides resistance to switching-currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.

Figure 4. Typical Connection Diagram (Internal Voltage Reference)



Notes: (1). Some modulators may require AC coupling capacitors (10μF).

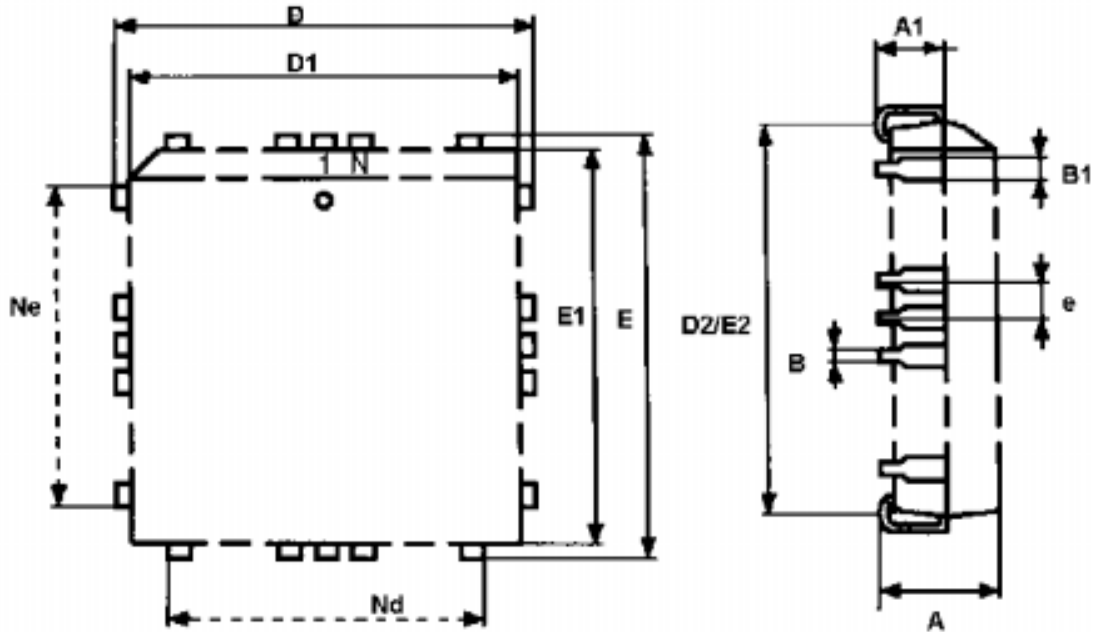
(2). Optional for chroma boost.

(3). VREFIN must be connected to either VREFOUT or VBIAS.

Table 6. Typical Parts List (Internal Voltage Reference)

Locations	Description	Vendor Part Number
C5 - 1, C7	0.1 μ F Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	47 μ F Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
L2, L3	Ferrite Bead($z < 300\Omega$ @ 5MHz)	ATC LCB0805, Taiyo Yuden BK2125LM182
RESET	1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)
<p>Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect SPCA711A performance.</p>		

PACKAGE INFORMATION



Model Number	Package	Ambient Temperature Range
SPCA711A	32-pin PLCC	0°C - 70°C

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance to supply the best possible product

Symbol	inches			mm		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.1	-	0.14	2.54	-	3.56
A1	0.06	-	0.09	1.52	-	2.41
B	0.013	-	0.02	0.33	-	0.53
B1	0.026	-	0.03	0.66	-	0.81
D	0.485	-	0.49	12.3	-	12.57
D1	0.447	-	0.45	11.3	-	11.56
D2	0.39	-	0.43	9.91	-	10.92
E	0.585	-	0.59	14.8	-	15.11
E1	0.547	-	0.55	13.8	-	14.1
E2	0.49	-	0.53	12.5	-	13.46
e	-	0.05	-	-	1.27	-
N	-	-	-	-	32	-
Nd	-	-	-	-	7	-
Ne	-	-	-	-	9	-

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