CMOS LSI

LC75373E

Electronic Volume Control for Car Stereo Systems

Overview

The LC75373E is an electronic volume control that can implement volume, balance, fader, bass/treble + super bass, loudness, input switching, and input/output level control functions with a minimal number of external components.

Functions

- Volume: Provides 81 positions, from 0 dB to –79 dB (in 1-dB steps) and –∞. A balance function can be implemented by controlling the left and right channels independently.
- Fader: This function can attenuate either the rear or the front outputs over 16 positions. (From 0 to –20 dB in 2-dB steps, from –20 to –25 dB in one 5-dB step, from –25 to –45 dB in 10-dB steps, –60 dB, and –∞.)
- Bass/treble: Forms an NF-type tone control circuit with the addition of external capacitors. The base and treble controls each have 15 positions.
- Input gain: The input signal can be amplified from 0 dB to +18.75 dB in 1.25 dB steps.
- Output gain: One of two output of 0 dB and + 6.5 dB can be selected for fader output.
- Input switch: The signal can be selected from one of four inputs for each of the left and right channels.
- Super bass: The position of super bass can be controlled in 11 steps.

Features

- On-chip buffer amplifiers for a minimum of external components.
- Built-in reference voltage generation circuit
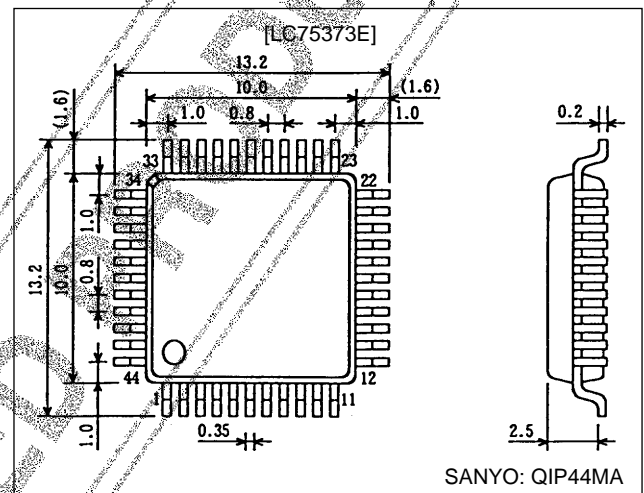- Serial data input: Supports CCB format communication with the system controller.

Package Dimensions

unit: mm

3148-QFP44MA

SANYO: QIP44MA

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		11	V
Maximum input voltage	V_{IN} max	CL, DI, CE		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–50 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LVRIN, RVRIN, L1 to L4, R1 to R4 LFIN, RFIN, LSIN, RSIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1			µs
Setup time	tsetup	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 8 V, V_{SS} = 0 V

| Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Maximum input gain	Gin max			+18.75		dB
Step resolution	Gstep			+1.25		dB
[Output Block]						
Maximum output gain	Gout max			+6.5		dB
[Volume Control Block]						
Step resolution	ATstep			1		dB
Step error	ATerr	step = 0 to −20 dB	−1	0	+1	dB
		step = −20 to −50 dB	−3	0	+3	dB
[Fader Volume Block]						
Step resolution	ATstep	step =0 to −20 dB		2		dB
		step = −20 to −25 dB		5		
		step = −25 to −45 dB		10		
Step error	ATerr	step = 0 to −45 dB	−2	0	+2	dB
		step = −45 to −60 dB	−3	0	+3	dB
Output load resistance	R_L		10			kΩ
[Bass/Treble Control Block]						
Bass control range	Gbass	Max. boost/cut	±9	±10.5	±12	dB
Treble control range	Gtre	Max. boost/cut	±8	±10.5	±13	dB
[Super Bass Block 1 (Type GEQ)]						
Control range	Crange	Max. boost		+17		dB
Step resolution	ATstep			+1.7		dB
[Super Bass Block 2 (Type T)]						
Control range	Crange	Max. boost		+20		dB
Step resolution	ATstep			+2.0		dB
[Overall Characteristics]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall		0.003	0.01	%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall, Rg = 1 kΩ		80.5		dB
Output at maximum attenuation	V_O min.	V_{IN} = 1 Vrms, f = 1 kHz, main volume at −∞		−80		dB
Output noise voltage	V_N1	All settings flat overall (IHF-A), Rg = 1 kΩ		8		µV
	V_N2	All settings flat overall (DIN-AUDIO), Rg = 1 kΩ		10		µV
Input high-level current	I_{IH}	CL, DI, CE: V_{IN} = 8 V			10	µA
Input low-level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	−10			µA

Note: Values in parenthesis are targets and will be fixed after evaluation.

Equivalent Circuit Block Diagram
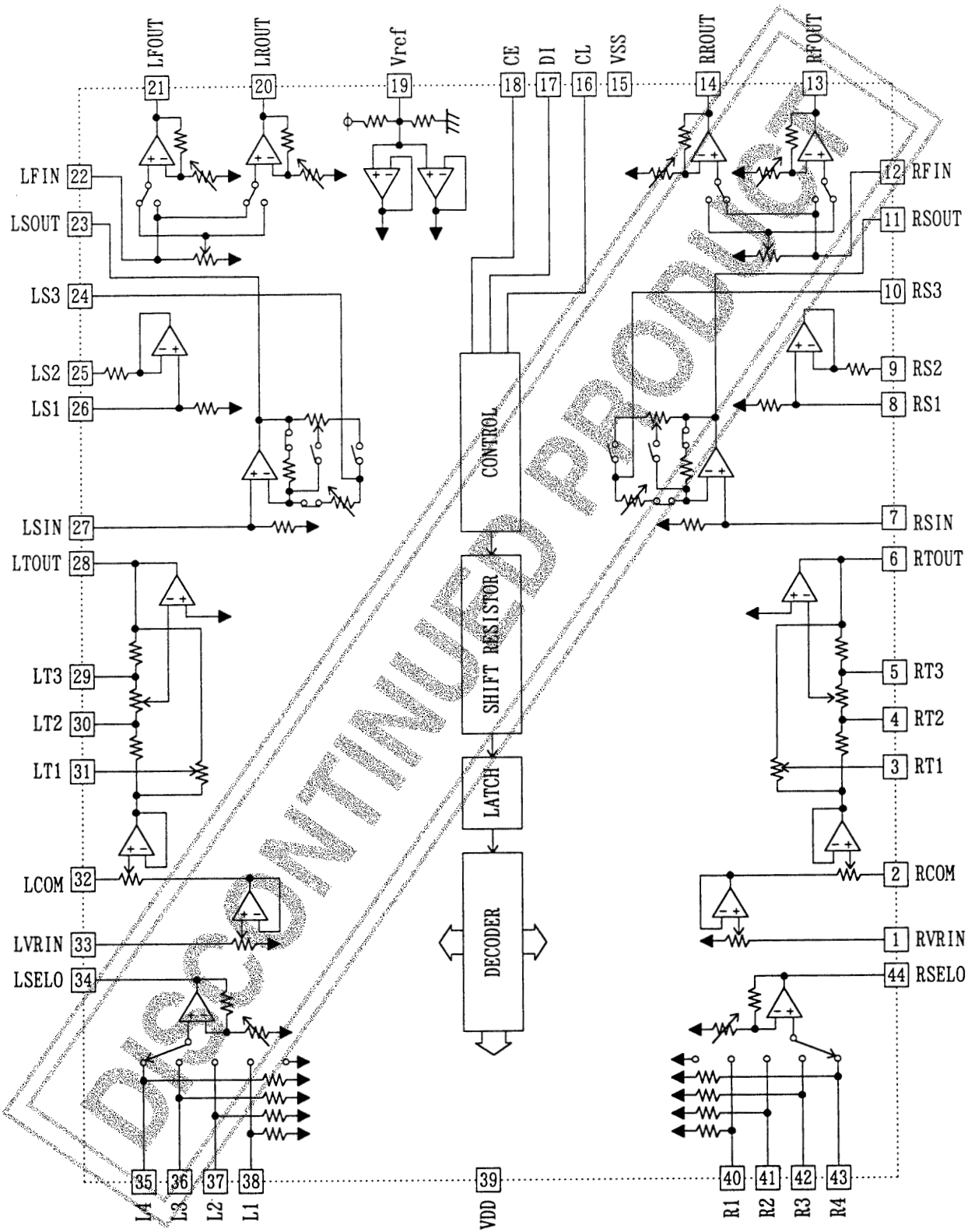
Sample Application Circuit
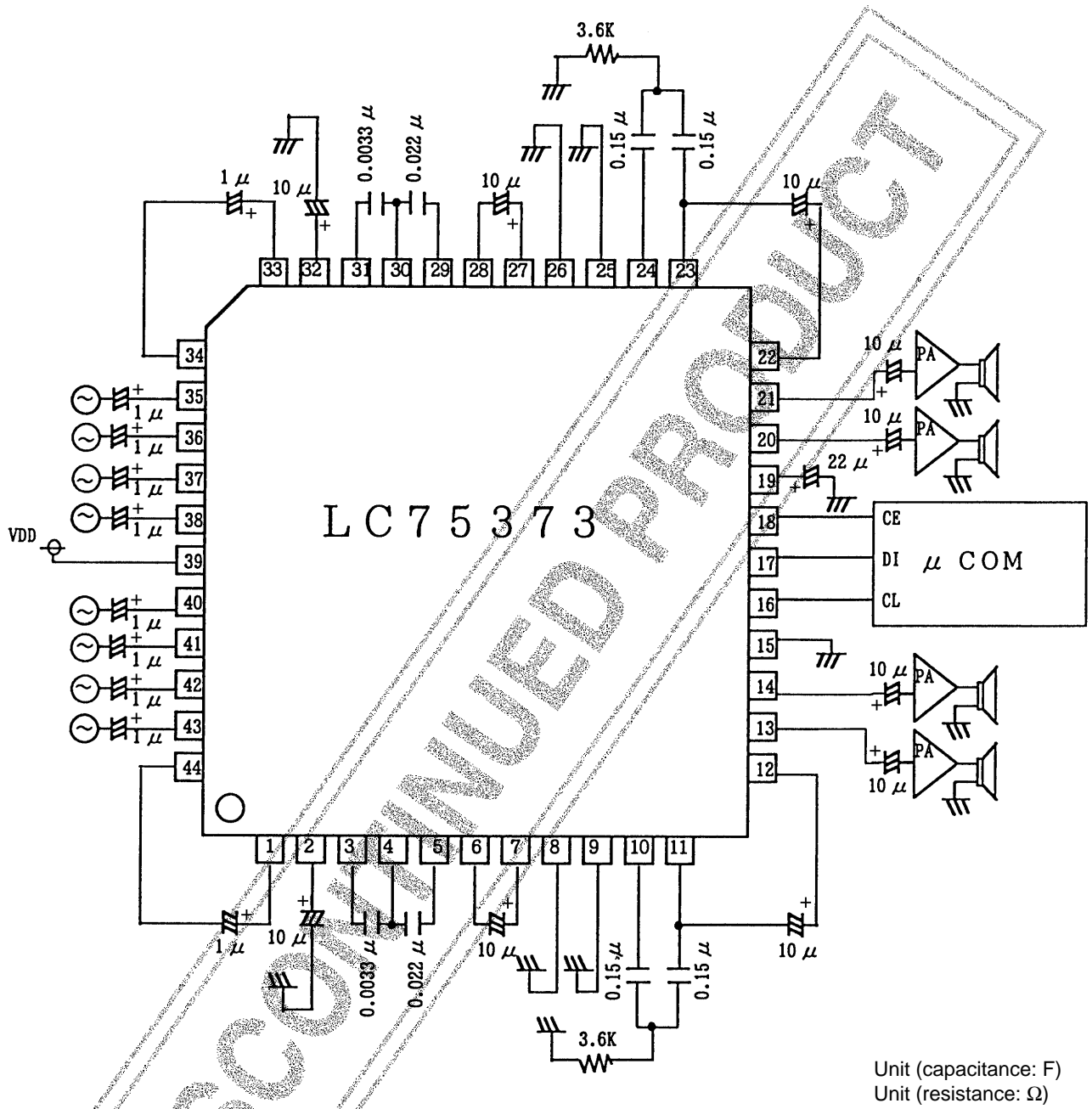
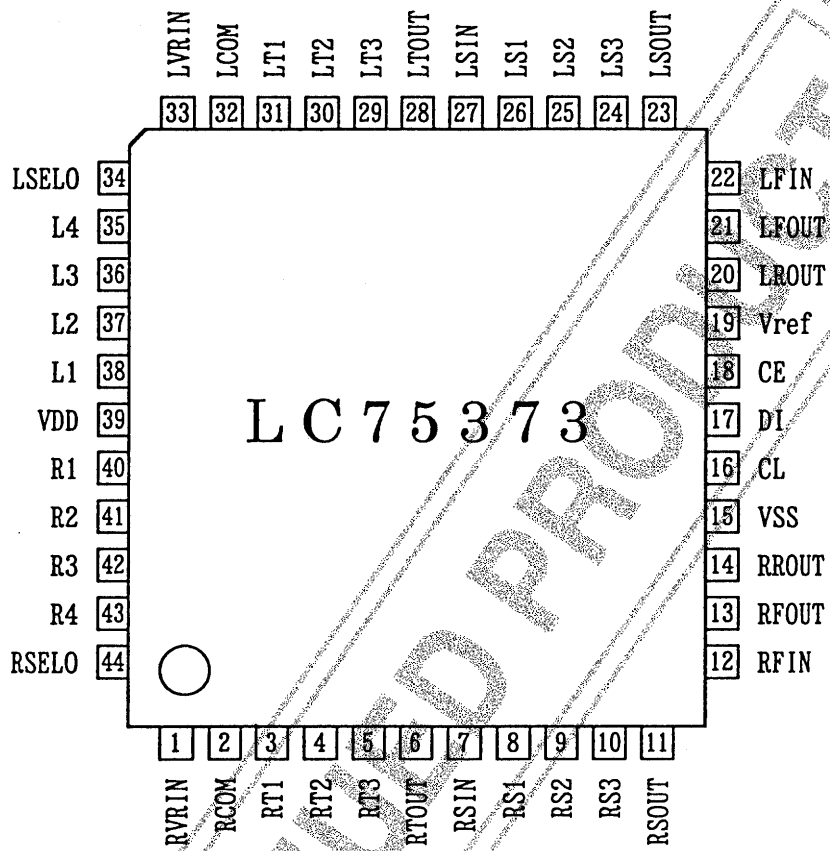1. When super bass circuit 1 (Type GEQ) is used
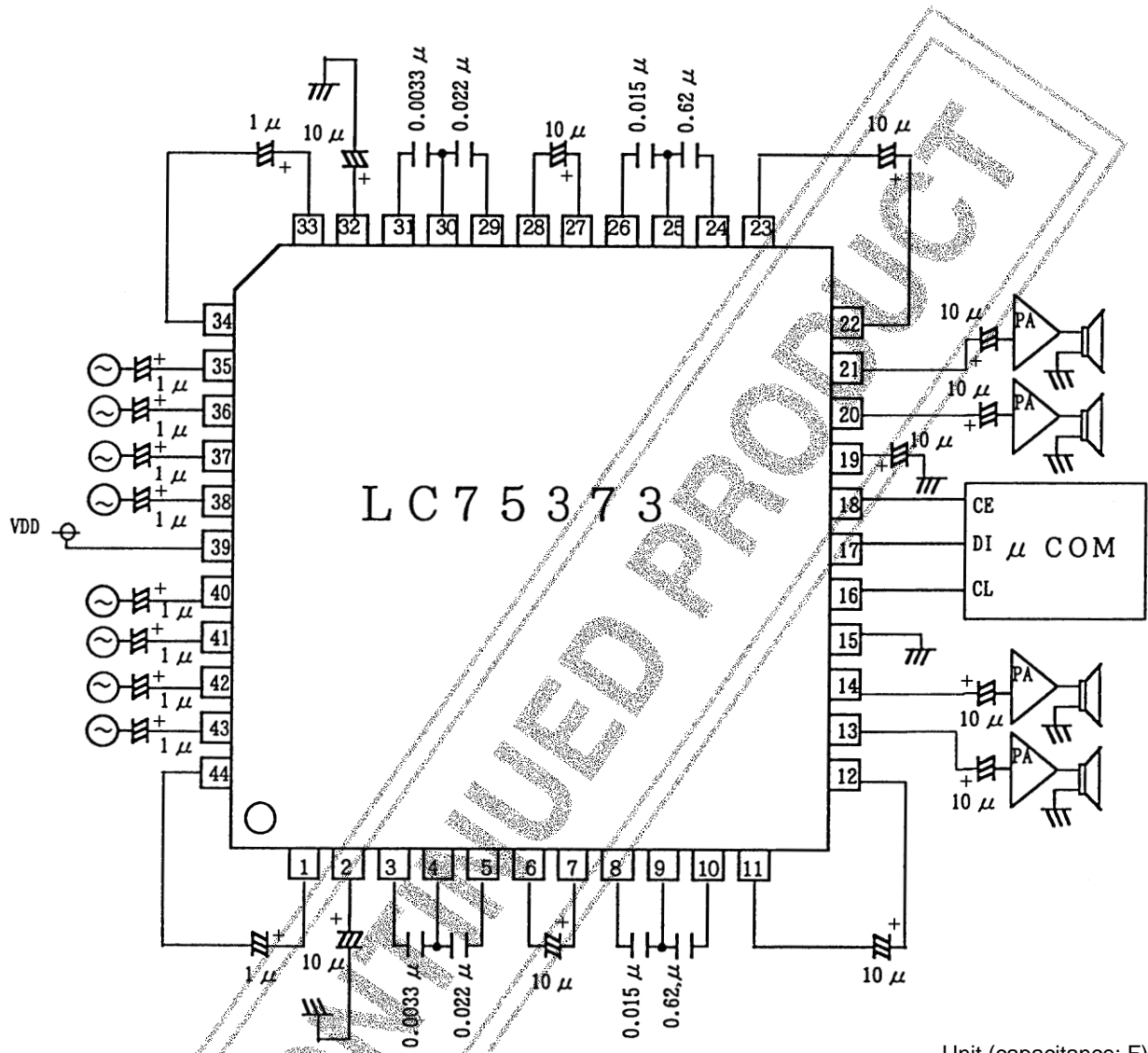
Unit (capacitance: F)

2. When super bass circuit 2 (Type T) is used

Unit (capacitance: F)
Unit (resistance: Ω)

Pin Assignment

Top view

Pin Functions

| Pin No.	Symbol	Function	Note
19	Vref	• 1/2 V_{DD} voltage generation block. A capacitor must be connected between Vref and V_{SS} to suppress power supply ripple.	
20 21 14 13	LROUT LFOUT RROUT RFOUT	• Fader outputs. The front and rear systems can be attenuated independently.	
22 12	LFIN RFIN	• Fader inputs • Must be driven from low-impedance circuits.	
28 6	LTOUT RTOUT	• Tone control outputs	
31 30 29 3 4 5	LT1 LT2 LT3 RT1 RT2 RT3	• Connections for the bass and treble compensation capacitors for the tone control circuit Connect high-band compensation capacitors between T1 and T2. Connect low-band compensation capacitors between T2 and T3.	
26 25 24 8 9 10	LS1 LS2 LS3 RS1 RS2 RS3	• Super bass compensation capacitors	
33 1	LVRIN RVRIN	• 4-dB volume control inputs • These inputs must be driven from low-impedance circuits.	

Continued from preceding page.

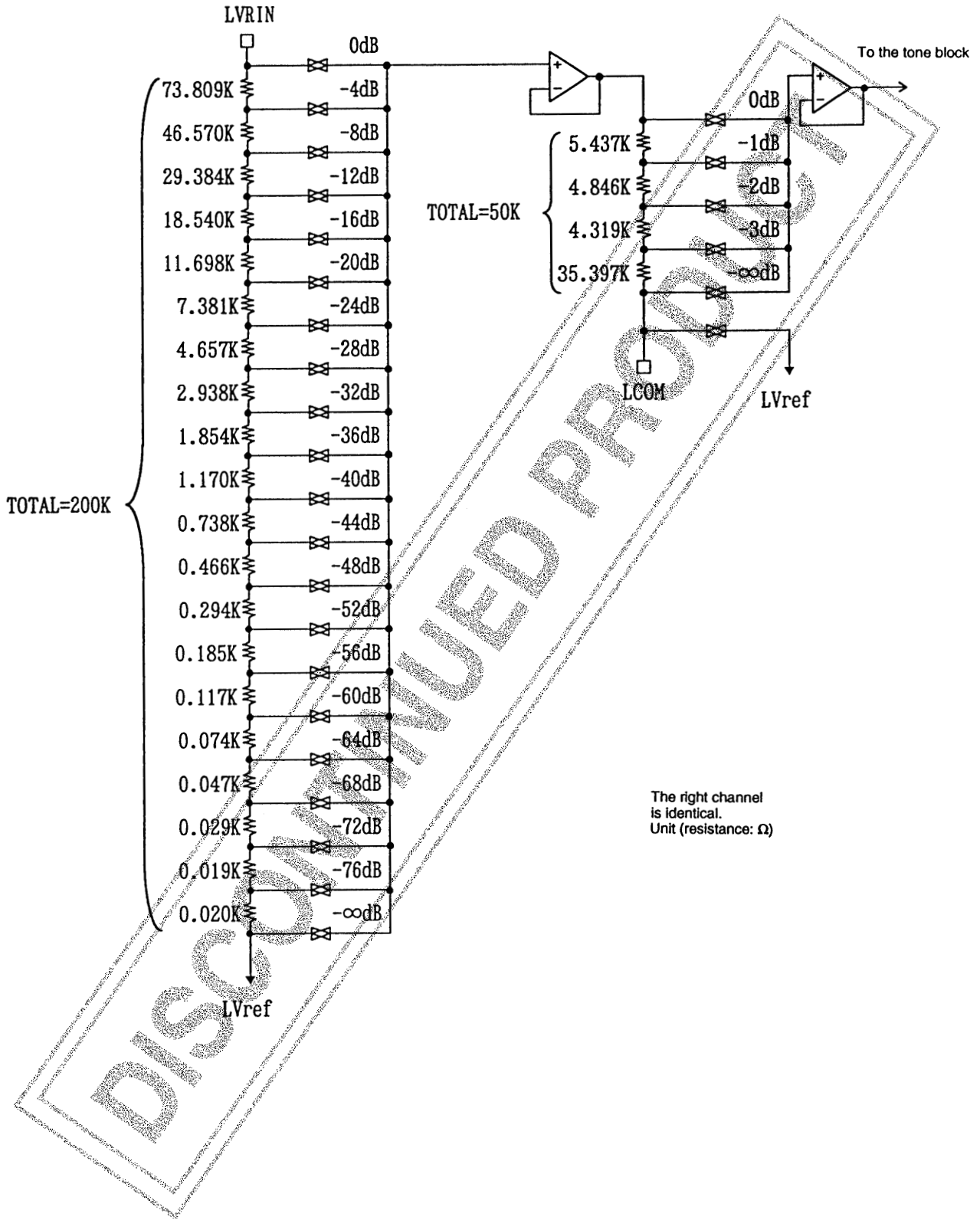| Pin No.	Symbol	Function	Note
34 44	LSELO RSELO	• Outputs from the input selector	
38 37 36 35 40 41 42 43	L1 L2 L3 L4 R1 R2 R3 R4	• Signal inputs	
39	V_{DD}	Power supply connection	
15	V_{SS}	Ground	
18	CE	Chip enable. Data is latched internally at the point this pin goes from high to low. The analog switches operate at that point. Data transfer is enabled when this pin is high.	
16 17	CL DI	Inputs for the serial data and clock used for LSI control.	
32 2	LCOM RCOM	1-dB block common outputs	
27 7	LSIN RSIN	• Super bass inputs • These inputs must be driven by low-impedance circuits.	
11 23	RSOUT LSOUT	• Super bass outputs	

Input Block Equivalent Circuit
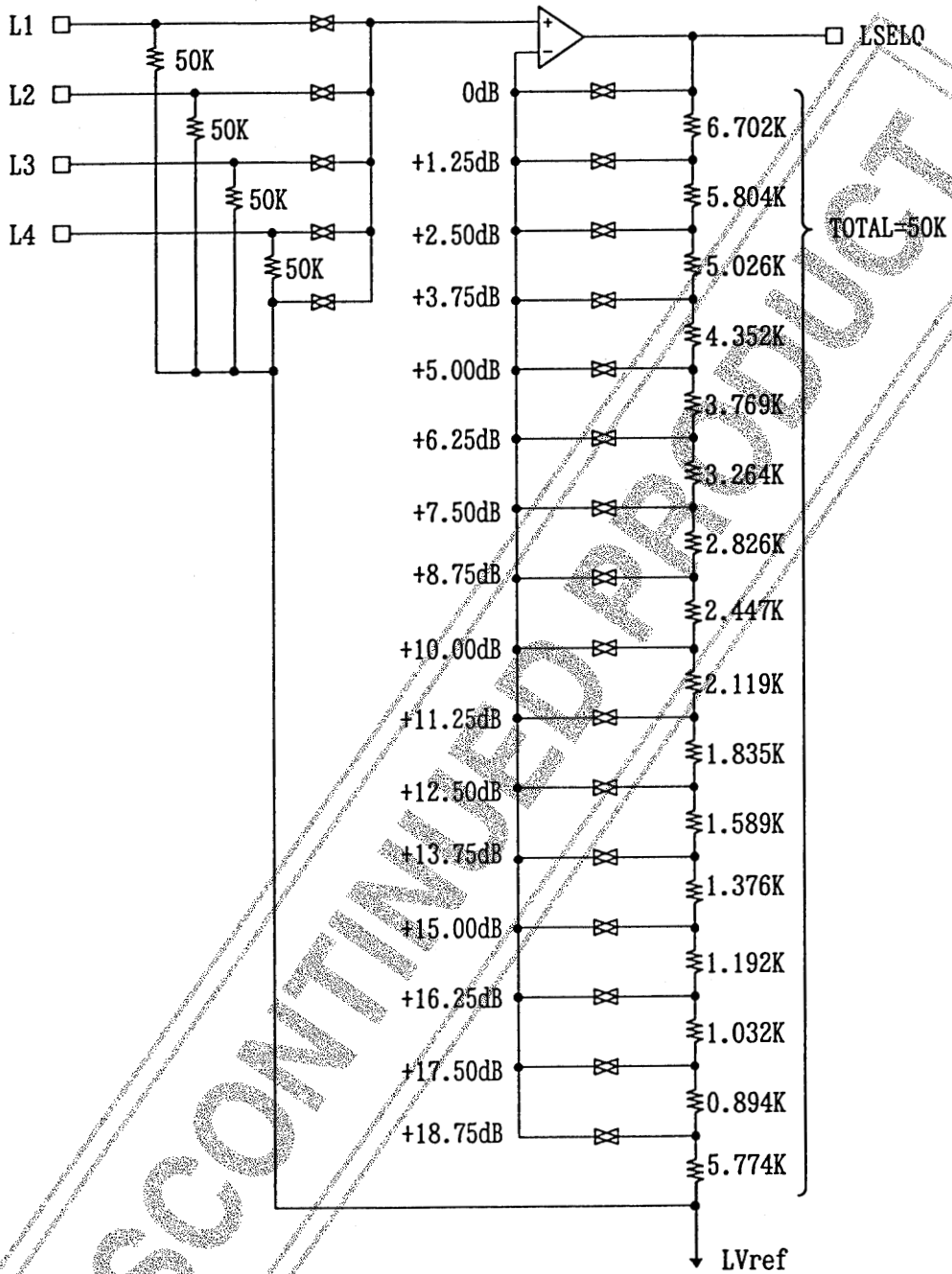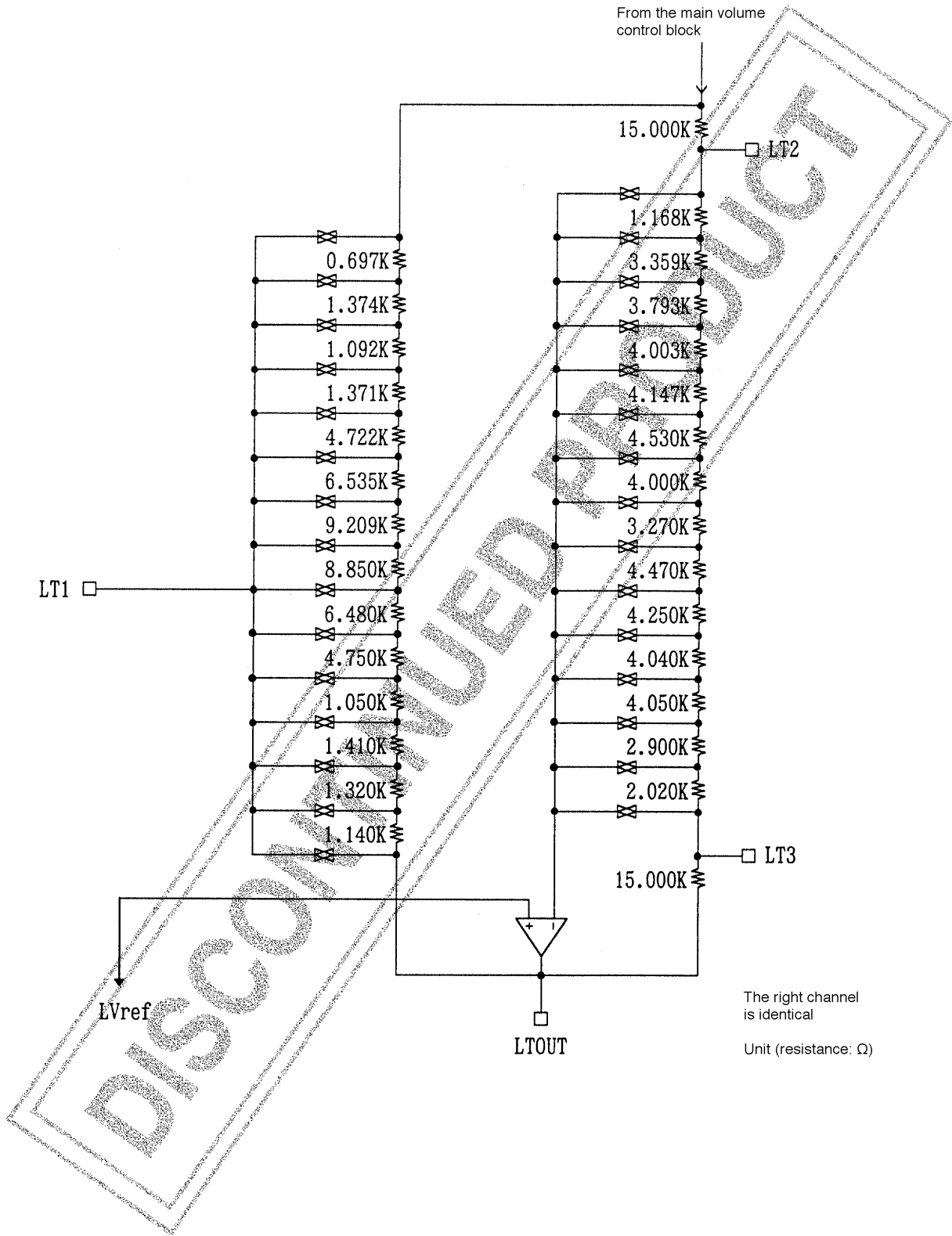

The right channel is identical.

Unit (resistance: Ω)

Main Volume Control Equivalent Circuit

LVRIN

0dB

73.809K   −4dB
46.570K   −8dB
29.384K   −12dB
18.540K   −16dB
11.698K   −20dB
7.381K   −24dB
4.657K   −28dB
2.938K   −32dB
1.854K   −36dB

TOTAL=200K

1.170K   −40dB
0.738K   −44dB
0.466K   −48dB
0.294K   −52dB
0.185K   −56dB
0.117K   −60dB
0.074K   −64dB
0.047K   −68dB
0.029K   −72dB
0.019K   −76dB
0.020K   −∞dB

LVref

TOTAL=50K

5.437K   0dB
4.846K   −1dB
4.319K   −2dB
35.397K   −3dB
           −∞dB

LCOM

LVref

To the tone block

The right channel is identical.
Unit (resistance: Ω)

Tone Control Block Equivalent Circuit

From the main volume control block

15.000K — LT2

1.168K
3.359K
3.793K
4.003K
4.147K
4.530K
4.000K
3.270K
4.470K
4.250K
4.040K
4.050K
2.900K
2.020K

0.697K
1.374K
1.092K
1.371K
4.722K
6.535K
9.209K
8.850K
LT1 — 6.480K
4.750K
1.050K
1.410K
1.320K
1.140K

LT3

15.000K

LVref

LTOUT

The right channel is identical

Unit (resistance: Ω)

## Super Bass Block Equivalent Circuit

Note: Concerning super bass switching control
• If the Q for super bass 1 (Type GEQ) is to be set to a relatively large value
SW1 ....on (Note that this switch should be set to the off position only if STEP 0 data was sent.)
SW2.............on
SW3.............off
SW4.............off
• If the Q for super bass 2 (Type I) can be set to a relatively small value without problem
SW1 ....off
SW2.............off
SW3.............on
SW4.............on

Super Bass Block Circuit 1 External Capacitor Calculation Example

The LC75373E external capacitors function as the structural elements for simulated inductances. This section presents the equivalent circuits and the formulas used to calculate the desired center frequencies.

Simulated Inductance Equivalent Circuit
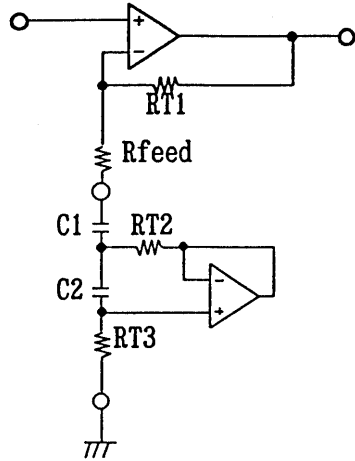
Sample Calculations

Specifications: Center frequency: F0 = 100 Hz
                   Q at maximum boost: Qmax = 1.05

① Determine the sharpness Q0 of the simulated inductance itself.
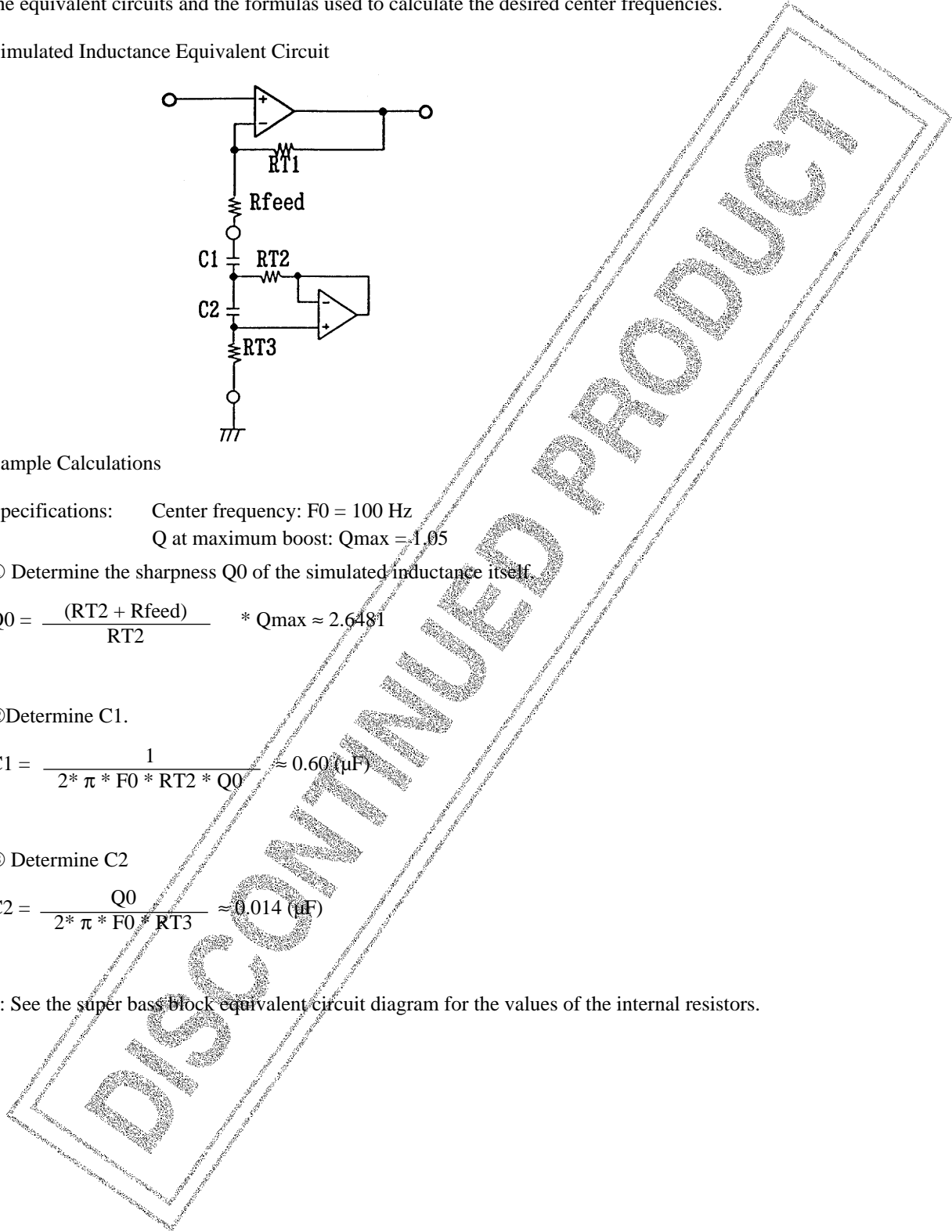
$$Q0 = \frac{(RT2 + Rfeed)}{RT2} * Qmax \approx 2.6481$$

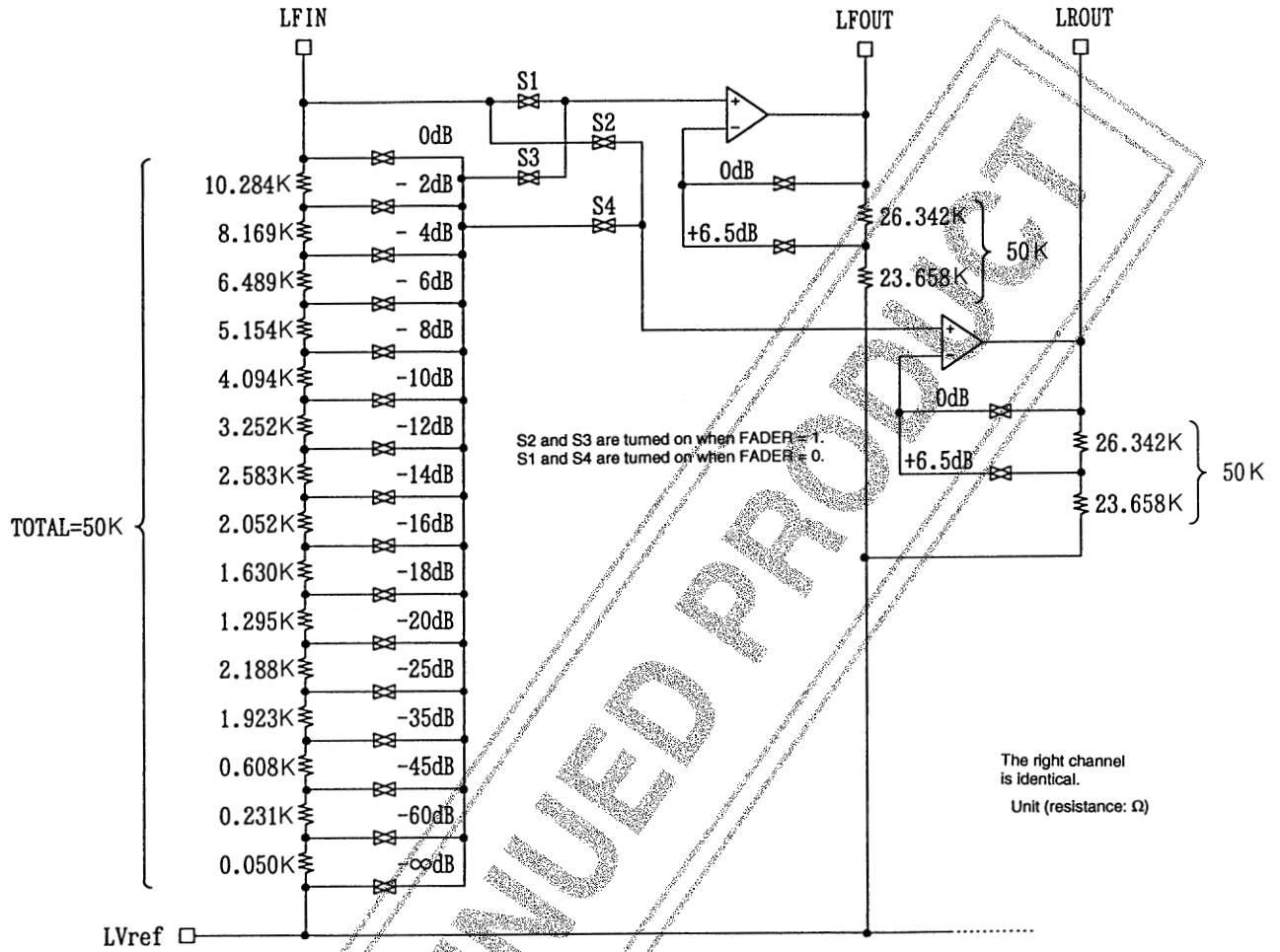②Determine C1.

$$C1 = \frac{1}{2*\pi*F0*RT2*Q0} \approx 0.60 \, (\mu F)$$

③ Determine C2

$$C2 = \frac{Q0}{2*\pi*F0*RT3} \approx 0.014 \, (\mu F)$$

*: See the super bass block equivalent circuit diagram for the values of the internal resistors.

Fader Volume Control Block Equivalent Circuit

S2 and S3 are turned on when FADER = 1.
S1 and S4 are turned on when FADER = 0.
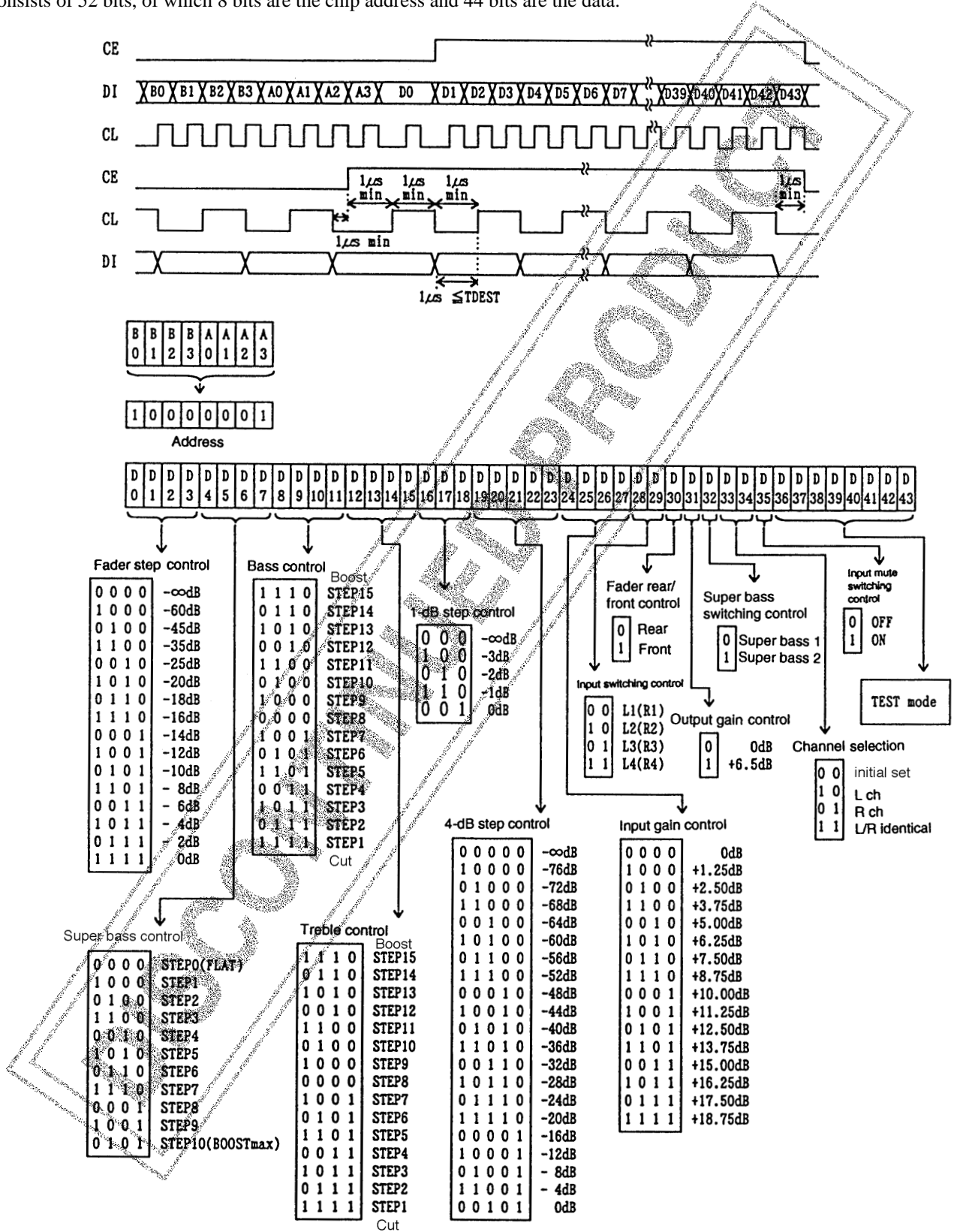
The right channel is identical.

Unit (resistance: Ω)

When data indicating an gain of −∞ is sent to the main volume control 1-dB step function, S1 and S2 open, and S3 and S4 go on at the same time.
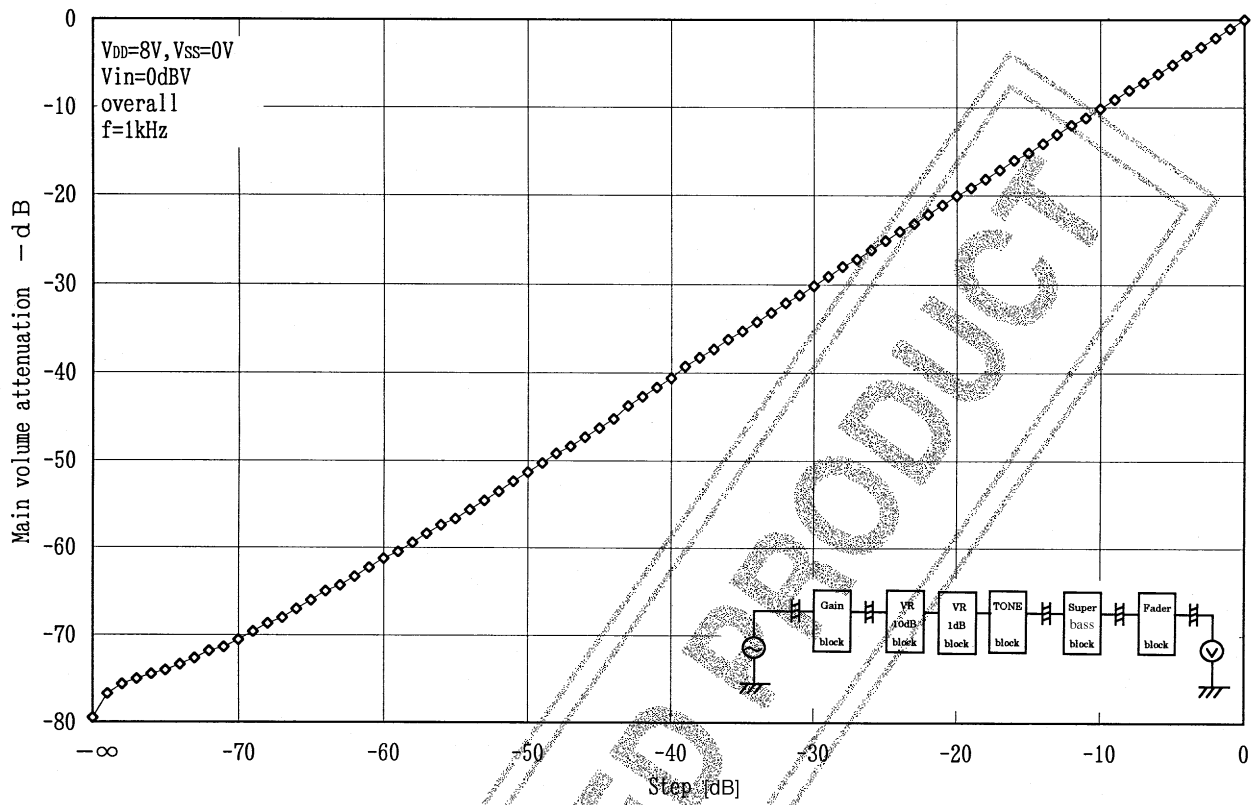
Control System Timing and Data Format

The LC75373E is controlled by applying serial data in the stipulated format to the CE, CL, and DI pins. The data consists of 52 bits, of which 8 bits are the chip address and 44 bits are the data.

Address

B0	B1	B2	B3	A0	A1	A2	A3
1	0	0	0	0	0	0	1

Fader step control

0 0 0 0	−∞dB
1 0 0 0	−60dB
0 1 0 0	−45dB
1 1 0 0	−35dB
0 0 1 0	−25dB
1 0 1 0	−20dB
0 1 1 0	−18dB
1 1 1 0	−16dB
0 0 0 1	−14dB
1 0 0 1	−12dB
0 1 0 1	−10dB
1 1 0 1	− 8dB
0 0 1 1	− 6dB
1 0 1 1	− 4dB
0 1 1 1	− 2dB
1 1 1 1	0dB

Bass control

		Boost
1 1 1 0	STEP15
0 1 1 0	STEP14
1 0 1 0	STEP13
0 0 1 0	STEP12
1 1 0 0	STEP11
0 1 0 0	STEP10
1 0 0 0	STEP9
0 0 0 0	STEP8
1 0 0 1	STEP7
0 1 0 1	STEP6
1 1 0 1	STEP5
0 0 1 1	STEP4
1 0 1 1	STEP3
0 1 1 1	STEP2
1 1 1 1	STEP1
	Cut

1-dB step control

0 0 0	−∞dB
1 0 0	−3dB
0 1 0	−2dB
1 1 0	−1dB
0 0 1	0dB

Fader rear/front control

0	Rear
1	Front

Input switching control

0 0	L1(R1)
1 0	L2(R2)
0 1	L3(R3)
1 1	L4(R4)

Super bass switching control

0	Super bass 1
1	Super bass 2

Output gain control

0	0dB
1	+6.5dB

Input mute switching control

0	OFF
1	ON

TEST mode

Channel selection

0 0	initial set
1 0	L ch
0 1	R ch
1 1	L/R identical

Super bass control

0 0 0 0	STEP0(FLAT)
1 0 0 0	STEP1
0 1 0 0	STEP2
1 1 0 0	STEP3
0 0 1 0	STEP4
1 0 1 0	STEP5
0 1 1 0	STEP6
1 1 1 0	STEP7
0 0 0 1	STEP8
1 0 0 1	STEP9
0 1 0 1	STEP10(BOOSTmax)

Treble control

		Boost
1 1 1 0	STEP15
0 1 1 0	STEP14
1 0 1 0	STEP13
0 0 1 0	STEP12
1 1 0 0	STEP11
0 1 0 0	STEP10
1 0 0 0	STEP9
0 0 0 0	STEP8
1 0 0 1	STEP7
0 1 0 1	STEP6
1 1 0 1	STEP5
0 0 1 1	STEP4
1 0 1 1	STEP3
0 1 1 1	STEP2
1 1 1 1	STEP1
	Cut

4-dB step control

0 0 0 0 0	−∞dB
1 0 0 0 0	−76dB
0 1 0 0 0	−72dB
1 1 0 0 0	−68dB
0 0 1 0 0	−64dB
1 0 1 0 0	−60dB
0 1 1 0 0	−56dB
1 1 1 0 0	−52dB
0 0 0 1 0	−48dB
1 0 0 1 0	−44dB
0 1 0 1 0	−40dB
1 1 0 1 0	−36dB
0 0 1 1 0	−32dB
1 0 1 1 0	−28dB
0 1 1 1 0	−24dB
1 1 1 1 0	−20dB
0 0 0 0 1	−16dB
1 0 0 0 1	−12dB
0 1 0 0 1	− 8dB
1 1 0 0 1	− 4dB
0 0 1 0 1	0dB

Input gain control

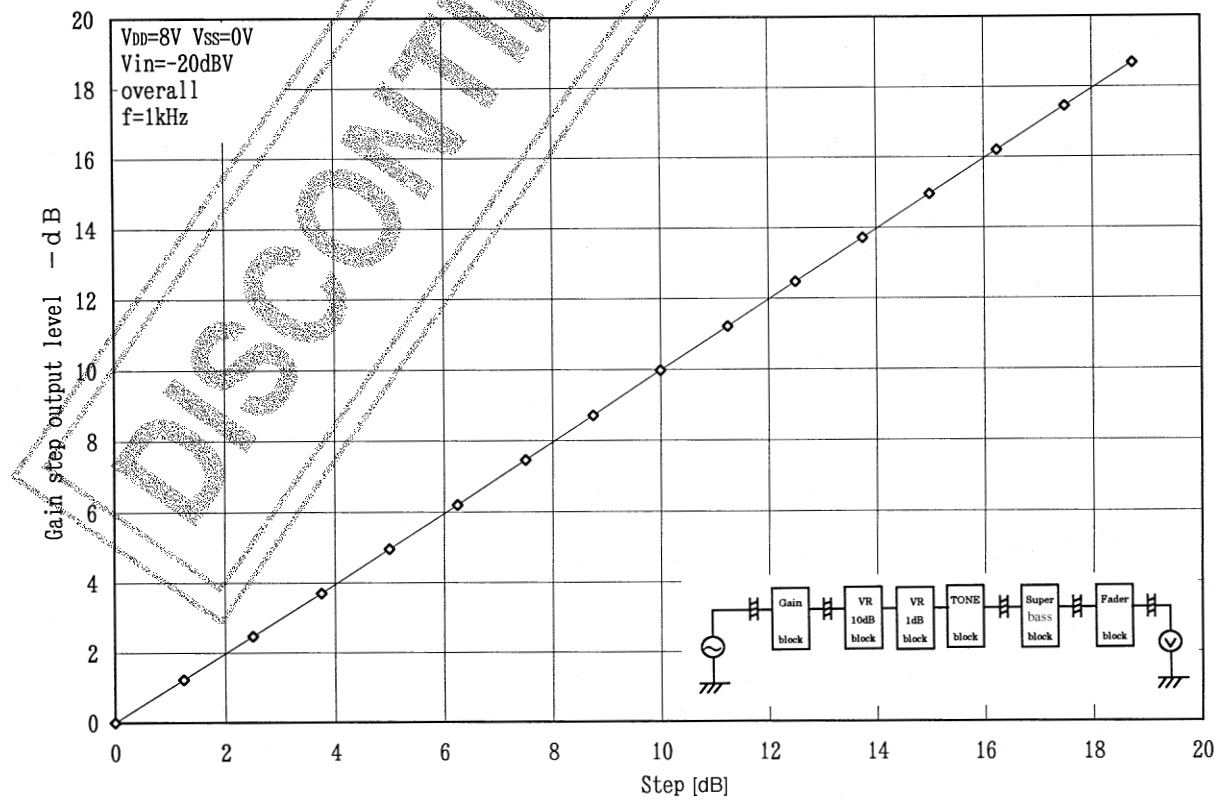|		
0 0 0 0	0dB
1 0 0 0	+1.25dB
0 1 0 0	+2.50dB
1 1 0 0	+3.75dB
0 0 1 0	+5.00dB
1 0 1 0	+6.25dB
0 1 1 0	+7.50dB
1 1 1 0	+8.75dB
0 0 0 1	+10.00dB
1 0 0 1	+11.25dB
0 1 0 1	+12.50dB
1 1 0 1	+13.75dB
0 0 1 1	+15.00dB
1 0 1 1	+16.25dB
0 1 1 1	+17.50dB
1 1 1 1	+18.75dB

Note: 1. The bits D36 to D43 are LSI test bits and must be set to 0.
   2. Concerning super bass switching
      If the Q for super bass 1 is to be set to a relatively large value
      If the Q for super bass 2 can be set to a relatively small value without problem

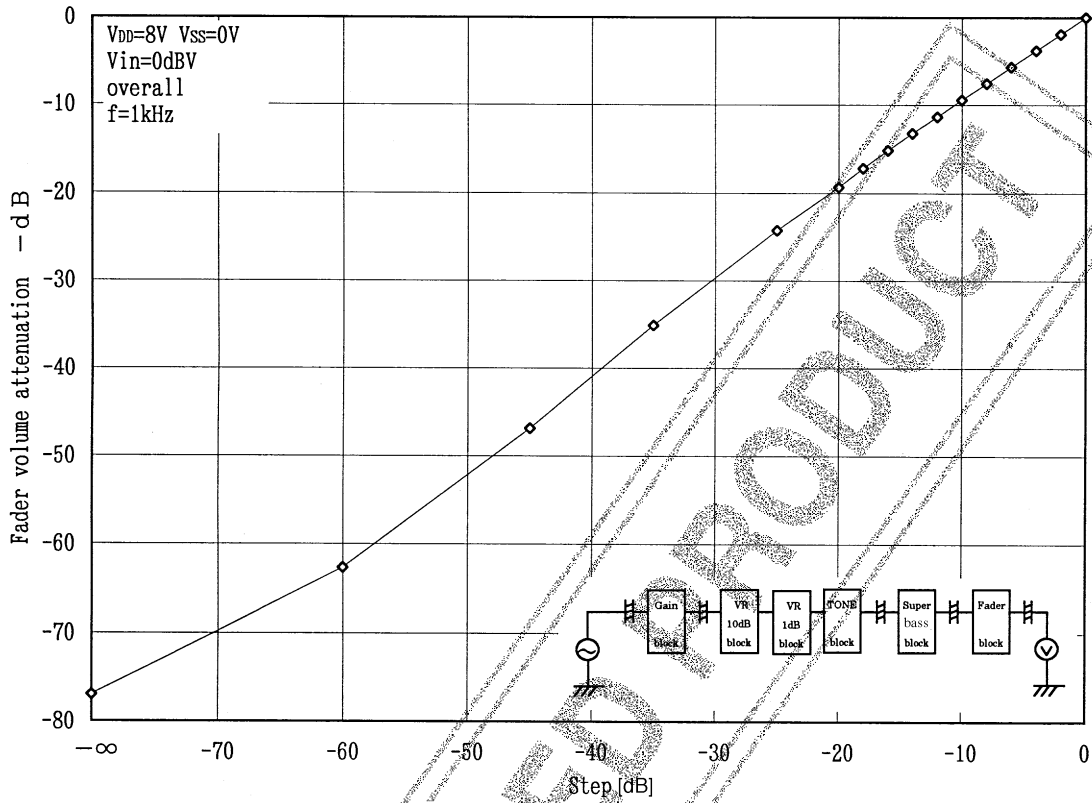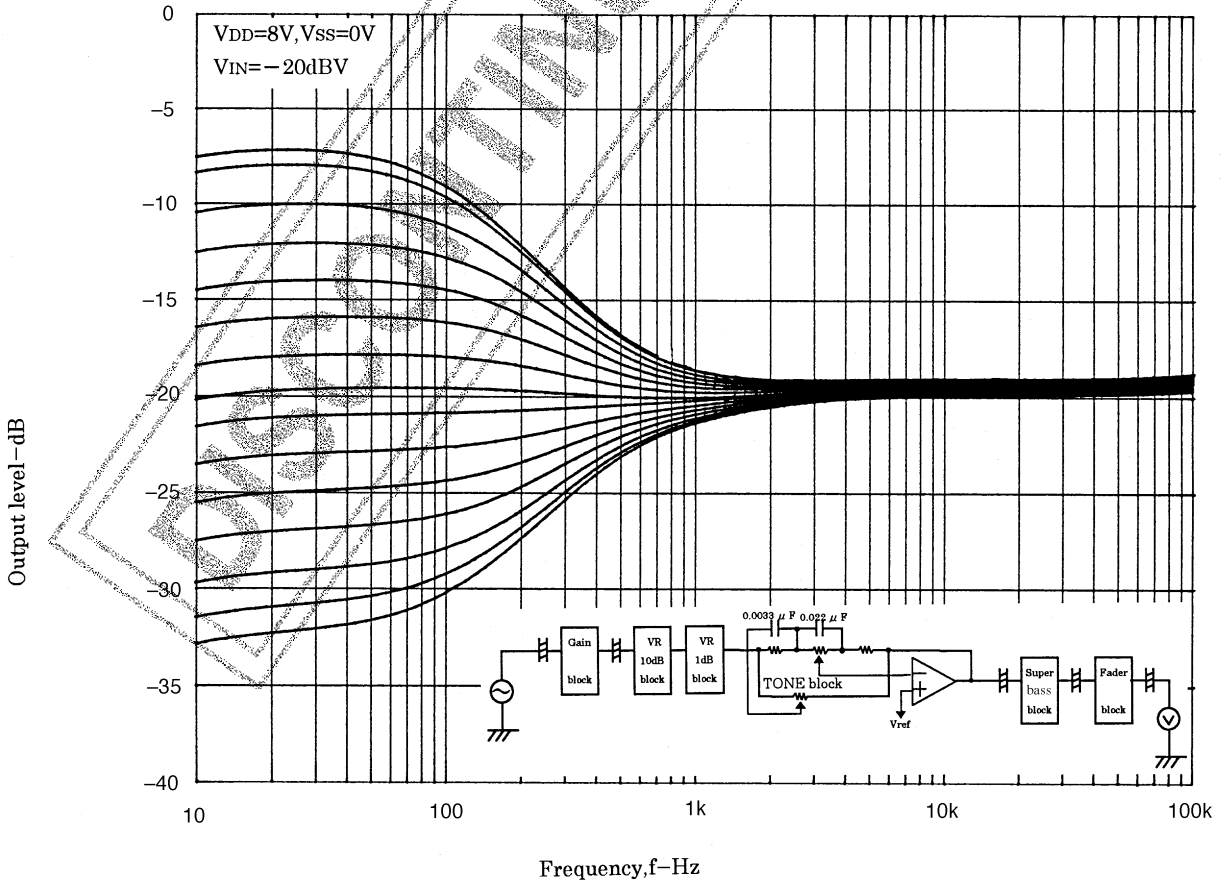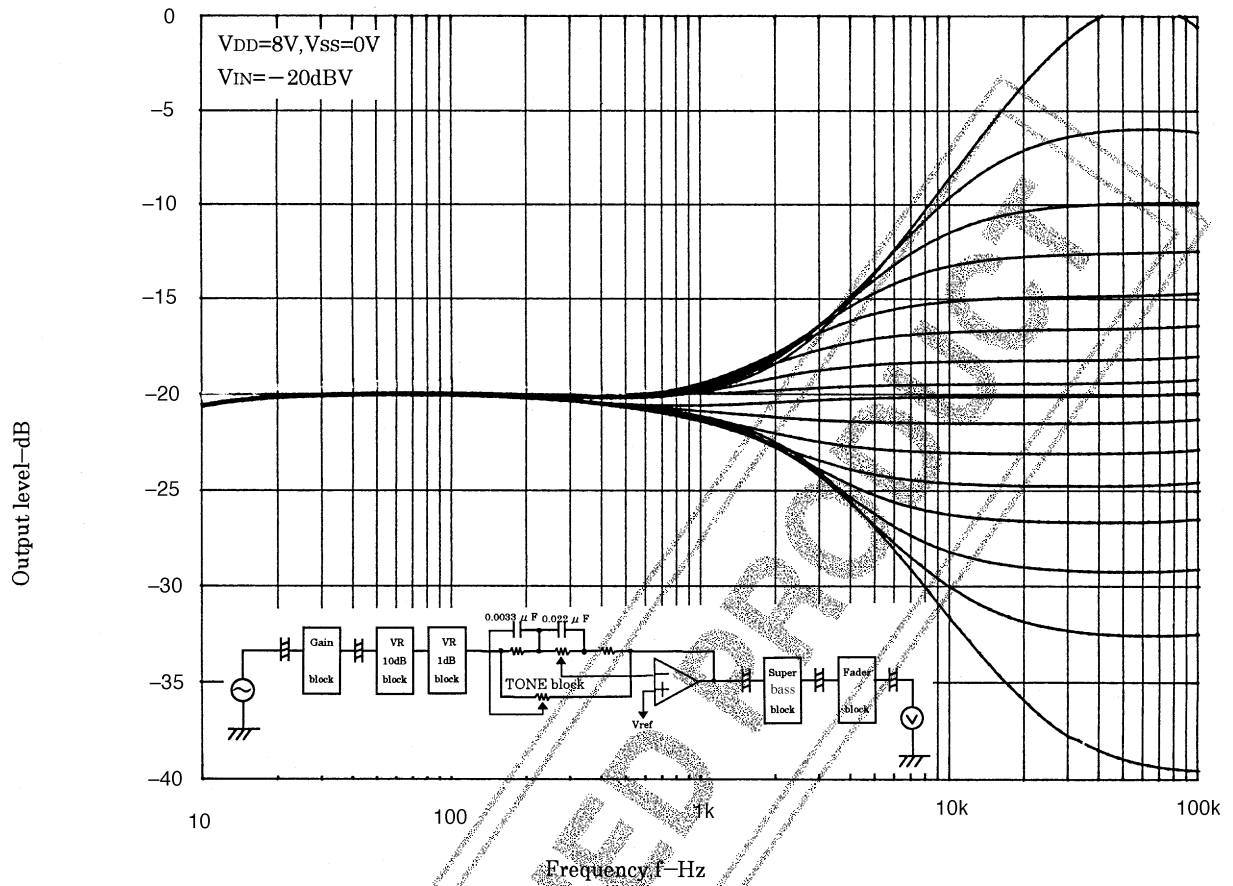## Main volume control characteristics

Main volume attenuation −dB vs Step [dB]

V_DD=8V, V_SS=0V
Vin=0dBV
overall
f=1kHz

Gain block / VR 10dB block / VR 1dB block / TONE block / Super bass block / Fader block

Gain step characteristics

Gain step output level −dB vs Step [dB]

V_DD=8V V_SS=0V
Vin=−20dBV
overall
f=1kHz

Gain block / VR 10dB block / VR 1dB block / TONE block / Super bass block / Fader block

Fader volume control step characteristics

V_DD=8V V_SS=0V
V_in=0dBV
overall
f=1kHz

Vertical axis: Fader volume attenuation −dB
Horizontal axis: Step [dB]

Bass control characteristics

V_DD=8V, V_SS=0V
V_IN=−20dBV

Vertical axis: Output level−dB
Horizontal axis: Frequency,f−Hz

Treble control characteristics

Frequency,f–Hz

Tone control characteristics
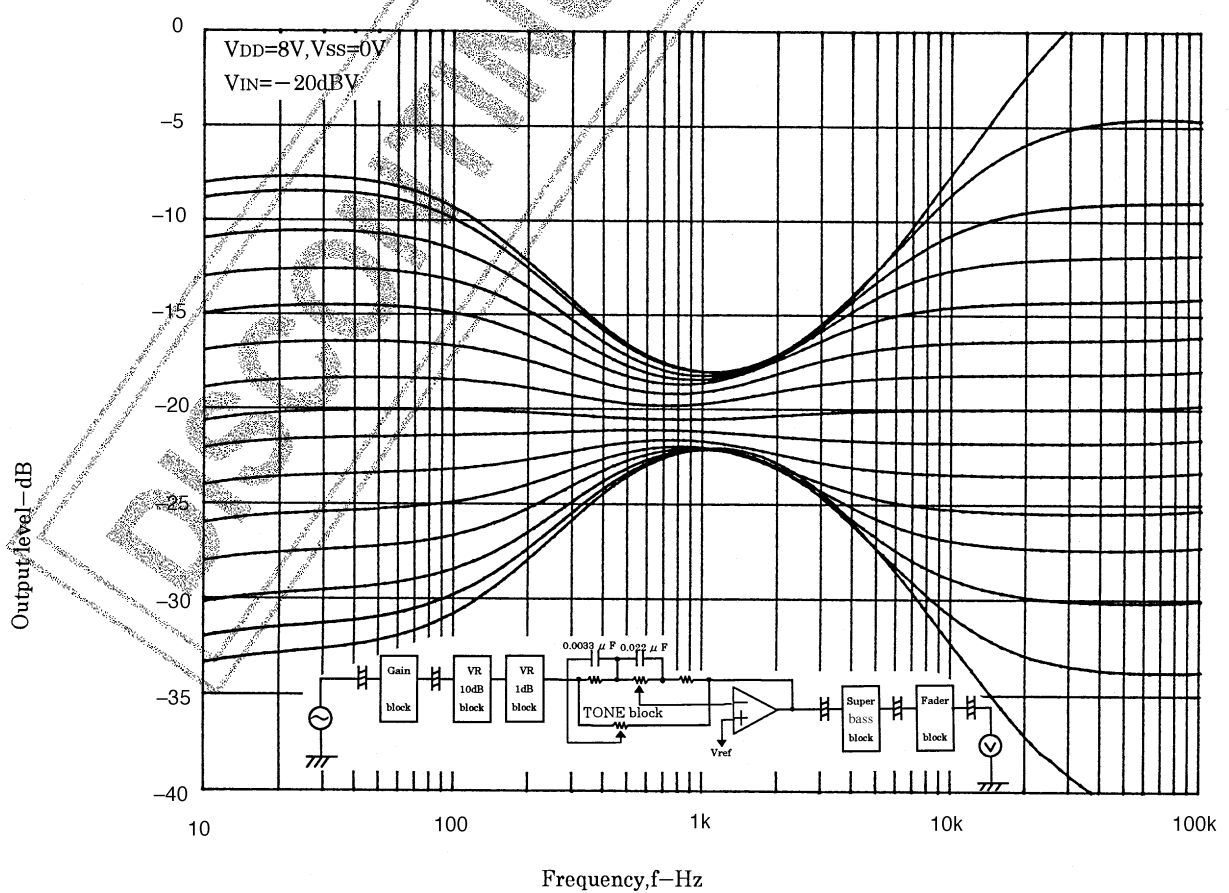
Frequency,f–Hz

Super bass 1 Type GEQ, control characteristics
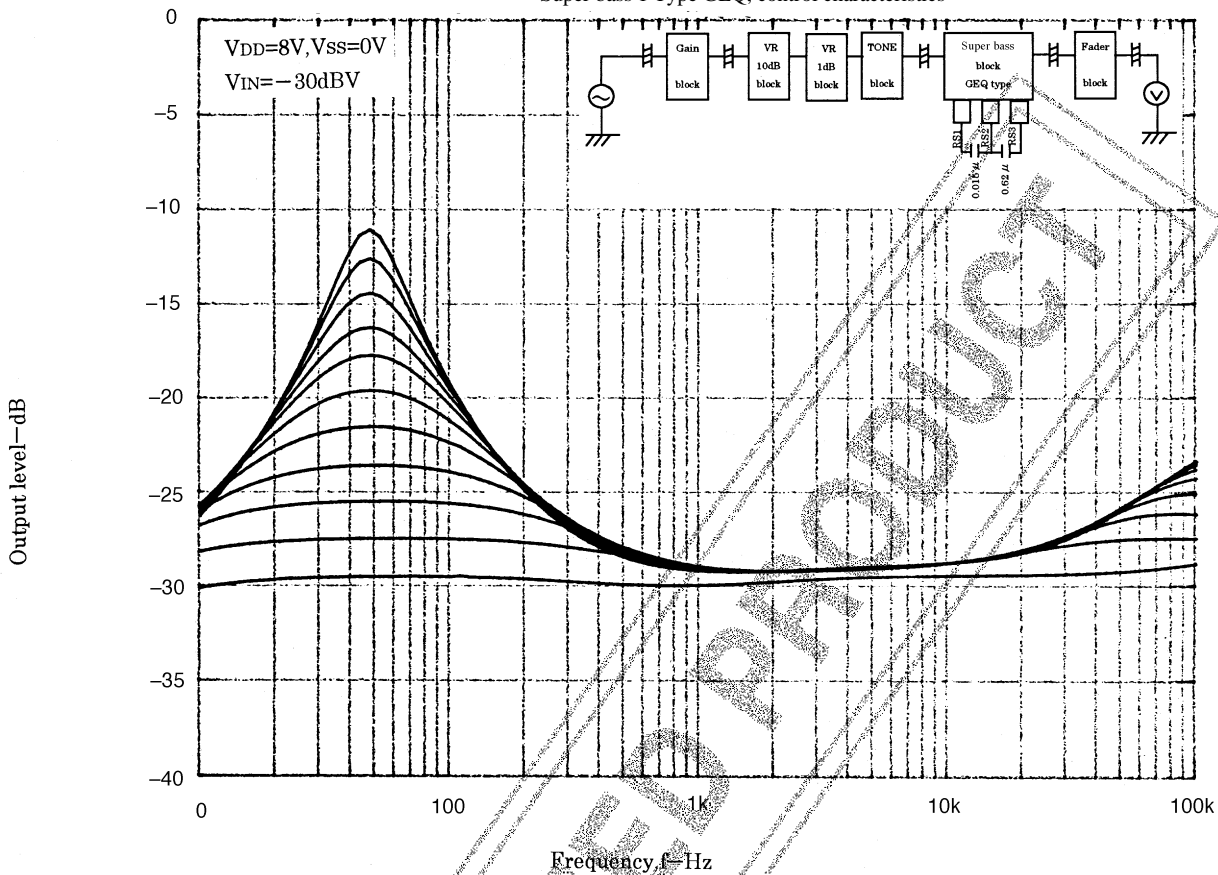
Super bass 2 Type T, control characteristics
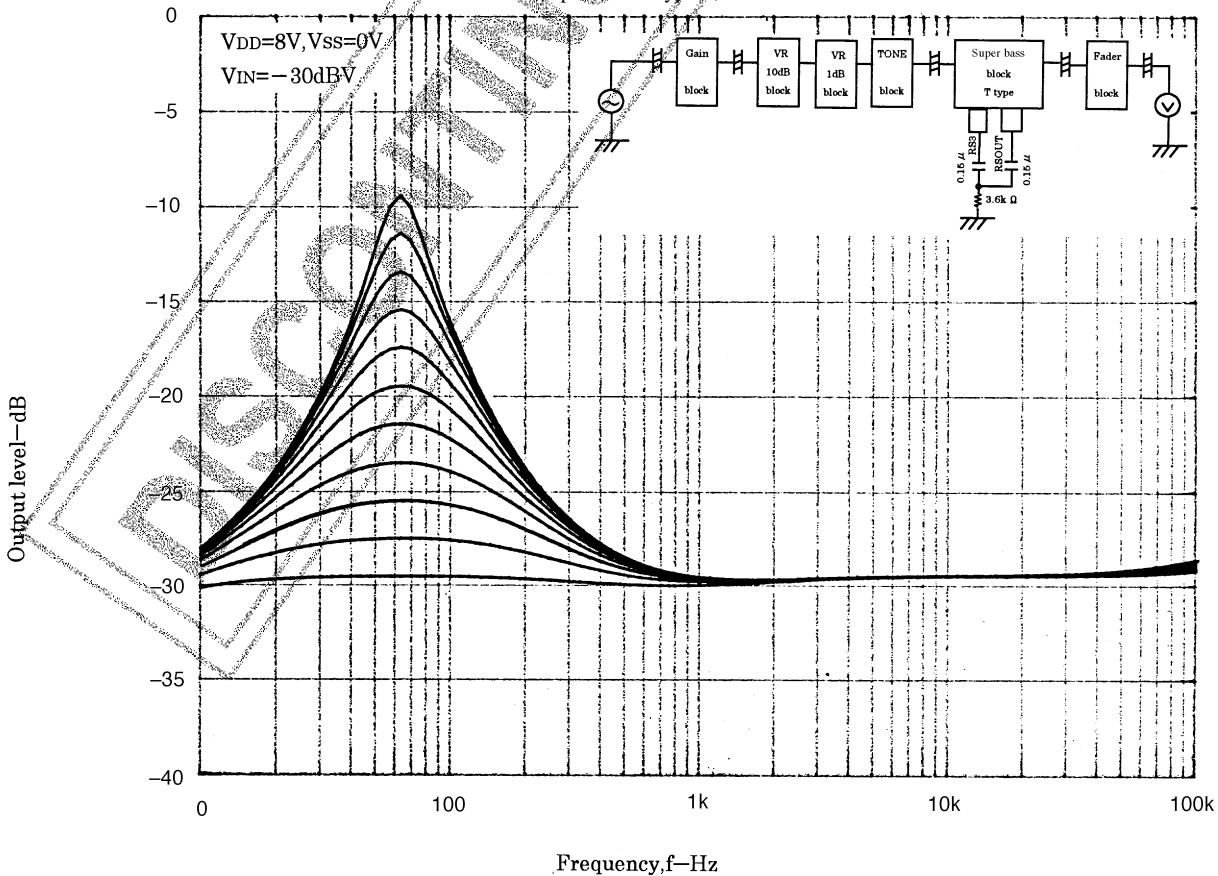
THD－Frequency characteristics
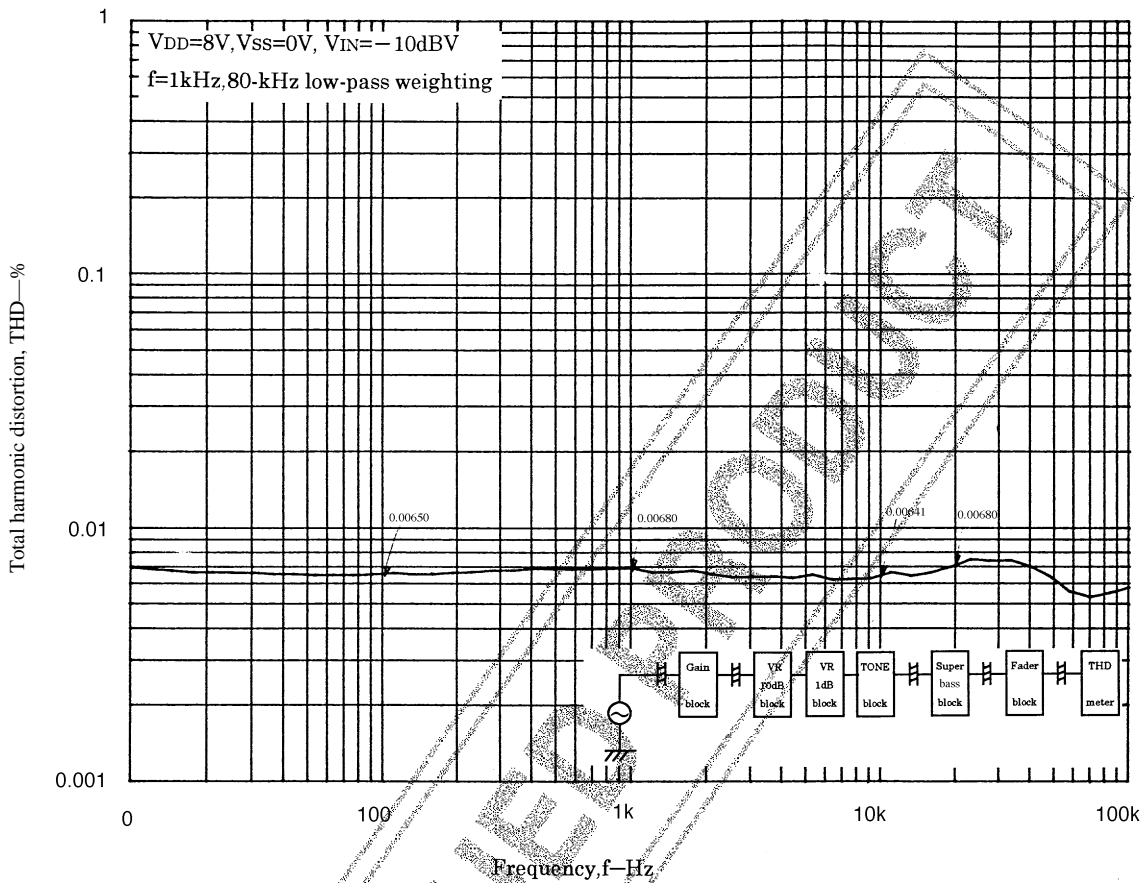
THD—Output level characteristics
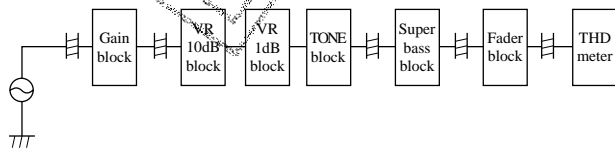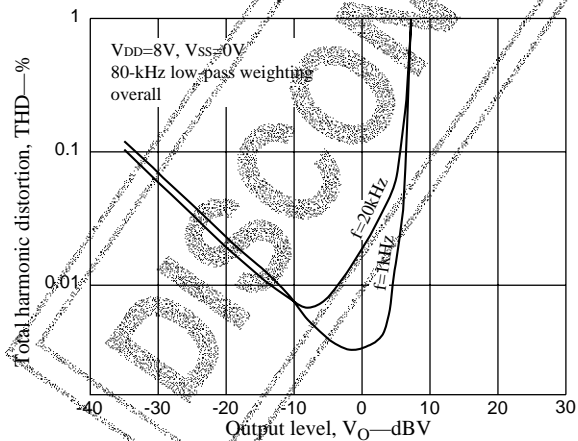
THD—Input level characteristics
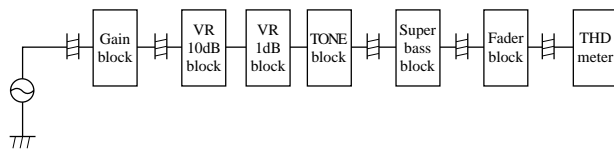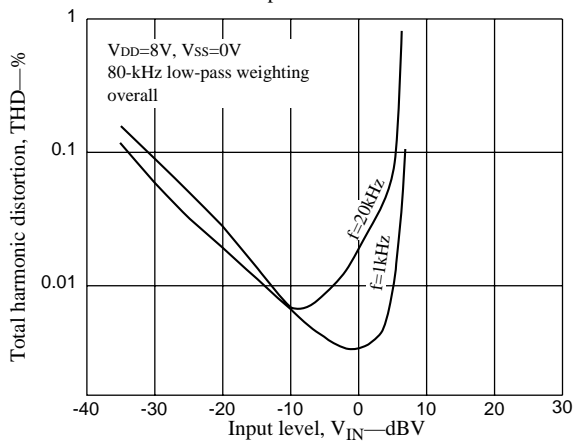
Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75373E.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.

This catalog provides information as of February, 1998. Specifications and information herein are subject to change without notice.